


# KR CS MLK 13" Schematics Whiskey Lake-U

2018-07-19  
REV: A00

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*DY : None Installed*  
*UMA: UMA only installed*

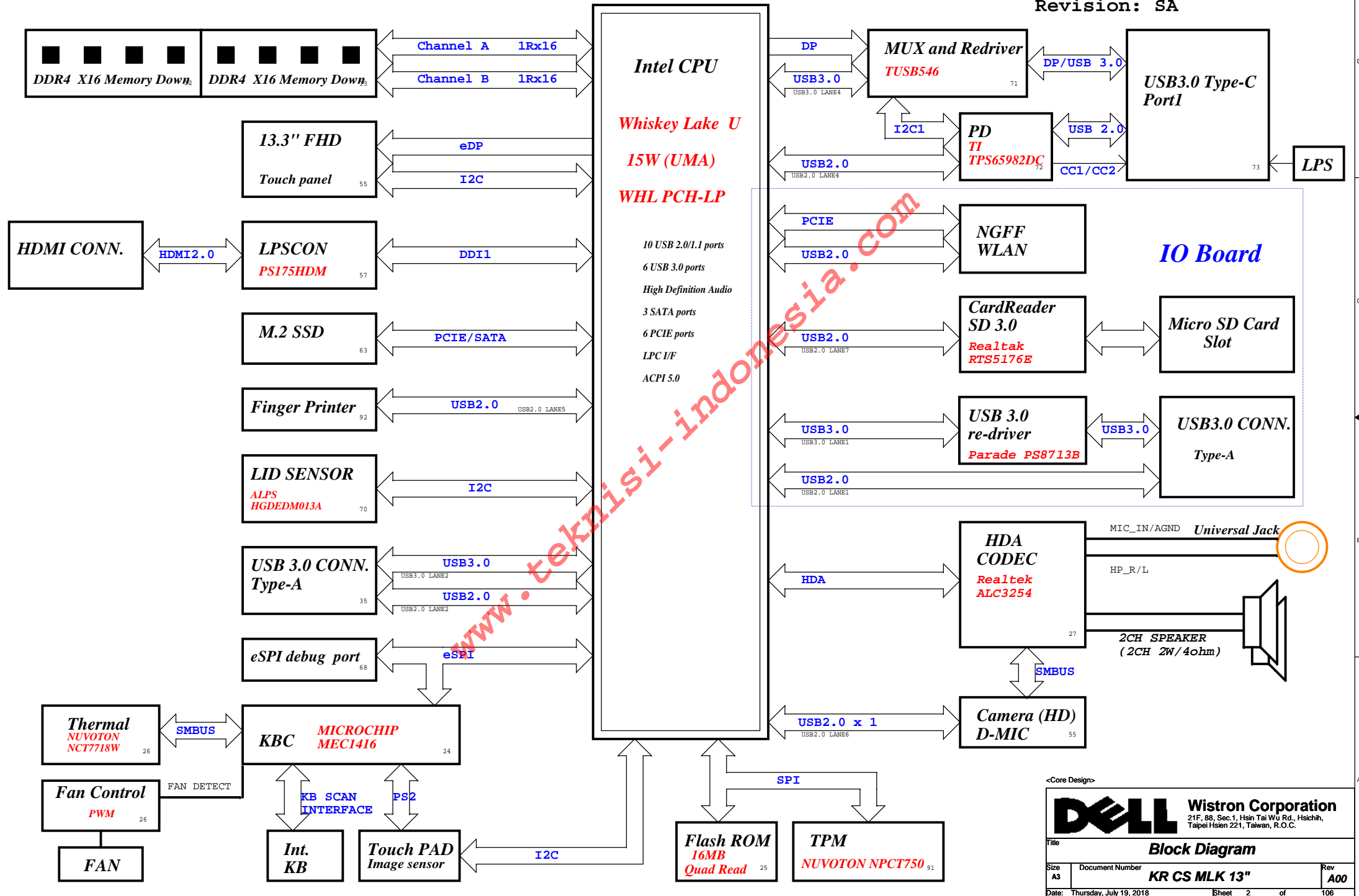
<Core Design>

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Title <b>Cover Page</b>		
Size A4	Document Number <b>KR CS MLK 13"</b>	Rev <b>A00</b>
Date: Thursday, July 19, 2018	Sheet 1 of	106



# WHL-U 13" CPU 15W Block Diagram

Project code: 4PD0EZ010001???  
PCB P/N: 17945  
Revision: SA









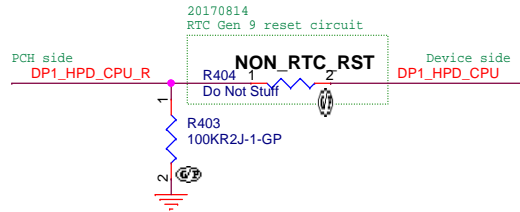
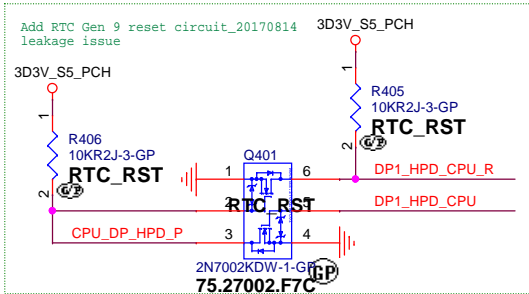
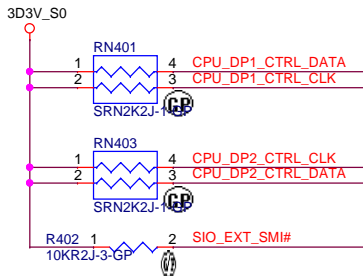
# SSID = CPU

## DP to HDMI2.0

[57] HDMI\_DDI\_TX\_N0 <<<  
[57] HDMI\_DDI\_TX\_P0 <<<  
[57] HDMI\_DDI\_TX\_N1 <<<  
[57] HDMI\_DDI\_TX\_P1 <<<  
[57] HDMI\_DDI\_TX\_N2 <<<  
[57] HDMI\_DDI\_TX\_P2 <<<  
[57] HDMI\_DDI\_TX\_N3 <<<  
[57] HDMI\_DDI\_TX\_P3 <<<  
[57] DP1\_AUX\_CPU\_N <<<  
[57] DP1\_AUX\_CPU\_P <<<  
[57] HDMI\_HPD\_CPU >>>

## DP for Type-C Mux

[71] DP2\_DDI\_TX\_N0 <<<  
[71] DP2\_DDI\_TX\_P0 <<<  
[71] DP2\_DDI\_TX\_N1 <<<  
[71] DP2\_DDI\_TX\_P1 <<<  
[71] DP2\_DDI\_TX\_N2 <<<  
[71] DP2\_DDI\_TX\_P2 <<<  
[71] DP2\_DDI\_TX\_N3 <<<  
[71] DP2\_DDI\_TX\_P3 <<<  
[71] DP2\_AUX\_CPU\_N <<<  
[71] DP2\_AUX\_CPU\_P <<<  
[55] eDP\_TX\_CPU\_N0 <<<  
[55] eDP\_TX\_CPU\_P0 <<<  
[55] eDP\_TX\_CPU\_N1 <<<  
[55] eDP\_TX\_CPU\_P1 <<<  
[55] eDP\_TX\_CPU\_N2 <<<  
[55] eDP\_TX\_CPU\_P2 <<<  
[55] eDP\_TX\_CPU\_N3 <<<  
[55] eDP\_TX\_CPU\_P3 <<<  
[55] eDP\_AUX\_CPU\_N <<<  
[55] eDP\_AUX\_CPU\_P <<<  
[55] eDP\_HPD\_CPU <<<  
[71,72] DP1\_HPD\_CPU <<<  
[24] L\_BKLT\_EN <<<  
[55] L\_BKLT\_CTRL <<<  
[55] EDP\_VDD\_EN <<<  
[15] GPP\_H17\_STRAP >>>



### (#543016) DDI Disabling and Termination Guidelines

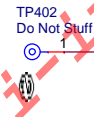
Port	Strap	Enable Port	Disable Port
Port 1	DDPB_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC
Port 2	DDPC_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC

## DP to HDMI2.0

## DP for Type-C Mux

1V\_VCCIO

CHECK WHL design guide: DISP\_RCOMP  
Design Guideline:  
Skylake processor signal eDP\_RCOMP should be connected to the VCCIO rail via a single 24.9 ±1% Q resistor



### (#543016) eDP\_RCOMP Guideline

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	20 mils	25 mils	24.9 Ω ±1%	Max = 100 mils

HDMI\_DDI\_TX\_N0 AL5  
HDMI\_DDI\_TX\_P0 AL6  
HDMI\_DDI\_TX\_N1 AJ5  
HDMI\_DDI\_TX\_P1 AJ6  
HDMI\_DDI\_TX\_N2 AF6  
HDMI\_DDI\_TX\_P2 AF5  
HDMI\_DDI\_TX\_N3 AE5  
HDMI\_DDI\_TX\_P3 AE6  
DP2\_DDI\_TX\_N0 AC4  
DP2\_DDI\_TX\_P0 AC3  
DP2\_DDI\_TX\_N1 AC1  
DP2\_DDI\_TX\_P1 AC2  
DP2\_DDI\_TX\_N2 AE4  
DP2\_DDI\_TX\_P2 AE3  
DP2\_DDI\_TX\_N3 AE1  
DP2\_DDI\_TX\_P3 AE2

CPU1A

1 OF 20

DDI1\_TXN0  
DDI1\_TXP0  
DDI1\_TXN1  
DDI1\_TXP1  
DDI1\_TXN2  
DDI1\_TXP2  
DDI1\_TXN3  
DDI1\_TXP3  
DDI2\_TXN0  
DDI2\_TXP0  
DDI2\_TXN1  
DDI2\_TXP1  
DDI2\_TXN2  
DDI2\_TXP2  
DDI2\_TXN3  
DDI2\_TXP3

EDP\_TXN0  
EDP\_TXP0  
EDP\_TXN1  
EDP\_TXP1  
EDP\_TXN2  
EDP\_TXP2  
EDP\_TXN3  
EDP\_TXP3

EDP\_AUX\_N  
EDP\_AUX\_P

DISP\_UTILS

DDI1\_AUX\_N  
DDI1\_AUX\_P  
DDI2\_AUX\_N  
DDI2\_AUX\_P  
DDI3\_AUX\_N  
DDI3\_AUX\_P

AG4 eDP\_TX\_CPU\_N0  
AG3 eDP\_TX\_CPU\_P0  
AG2 eDP\_TX\_CPU\_N1  
AG1 eDP\_TX\_CPU\_P1  
AJ4 eDP\_TX\_CPU\_N2  
AJ3 eDP\_TX\_CPU\_P2  
AJ2 eDP\_TX\_CPU\_N3  
AJ1 eDP\_TX\_CPU\_P3

AH4 eDP\_AUX\_CPU\_N  
AH3 eDP\_AUX\_CPU\_P

AM7

AC7 DP1\_AUX\_CPU\_N  
AC6 DP1\_AUX\_CPU\_P  
AD4 DP2\_AUX\_CPU\_N  
AD3 DP2\_AUX\_CPU\_P  
AG7  
AG6

20180208  
Follow RO NC

for HDMI2.0

for Type-C Mux

GPP\_E13/DDPB\_HPD0/DISP\_MISC0  
GPP\_E14/DDPC\_HPD1/DISP\_MISC1  
GPP\_E15/DPPD\_HPD2/DISP\_MISC2  
GPP\_E16/DPPPE\_HPD3/DISP\_MISC3  
GPP\_E17/EDP\_HPD/DISP\_MISC4

EDP\_BKLTEN  
EDP\_VDDEN  
EDP\_BKLTCTL

DISP\_RCOMP

GPP\_E18/DPPB\_CTRLCLK/CNV\_BT\_HOST\_WAKE#  
GPP\_E19/DPPB\_CTRLDATA

GPP\_E20/DPPC\_CTRLCLK  
GPP\_E21/DPPC\_CTRLDATA

GPP\_E22/DPPD\_CTRLCLK  
GPP\_E23/DPPD\_CTRLDATA

GPP\_H16/DDPF\_CTRLCLK  
GPP\_H17/DDPF\_CTRLDATA

WHISKEY-LAKE-GP

<Core Design>



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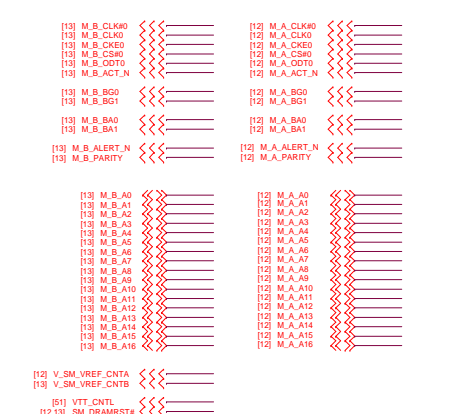
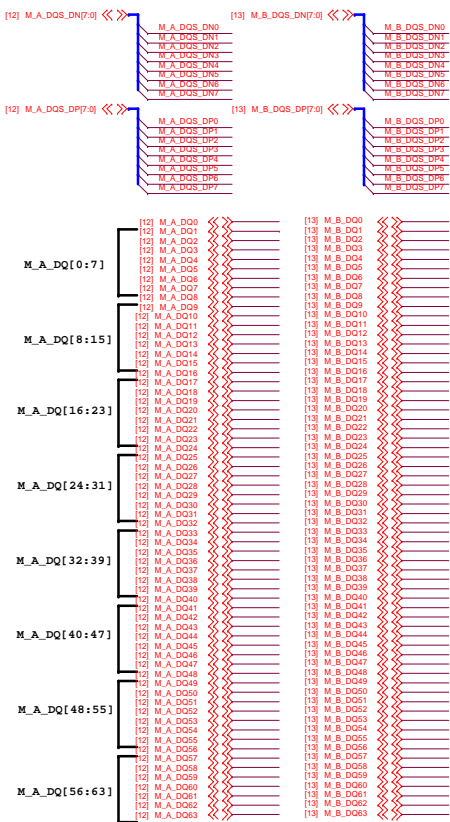
Title **CPU\_(JTAG/CPU SIDE BAND)**

Size Document Number **KR CS MLK 13"** Rev **A00**

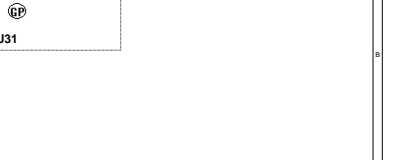
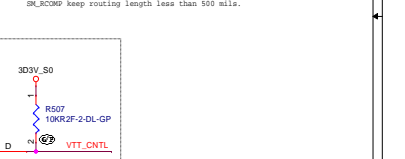
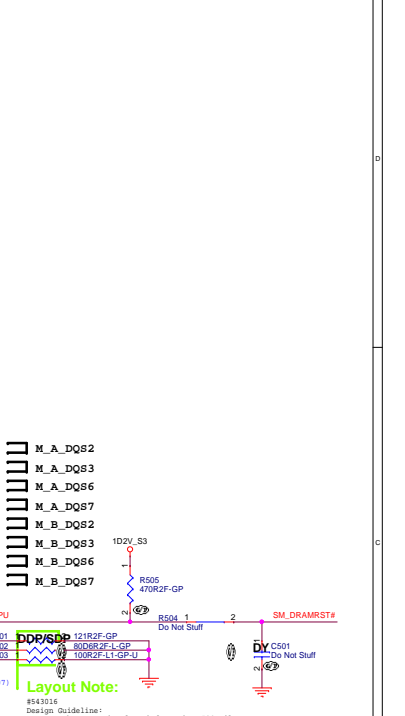
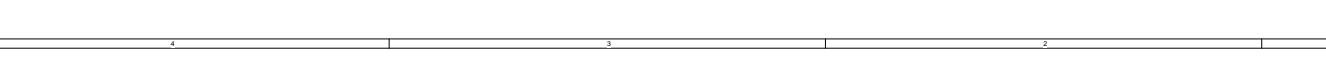
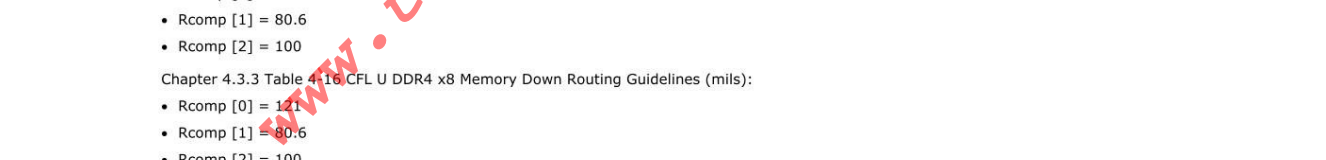
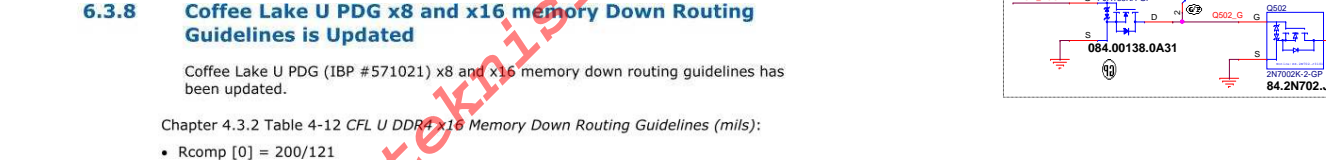
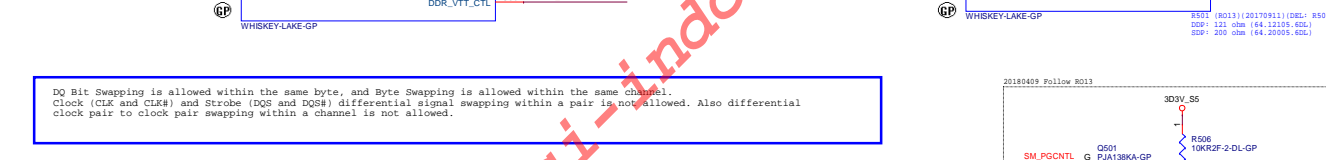
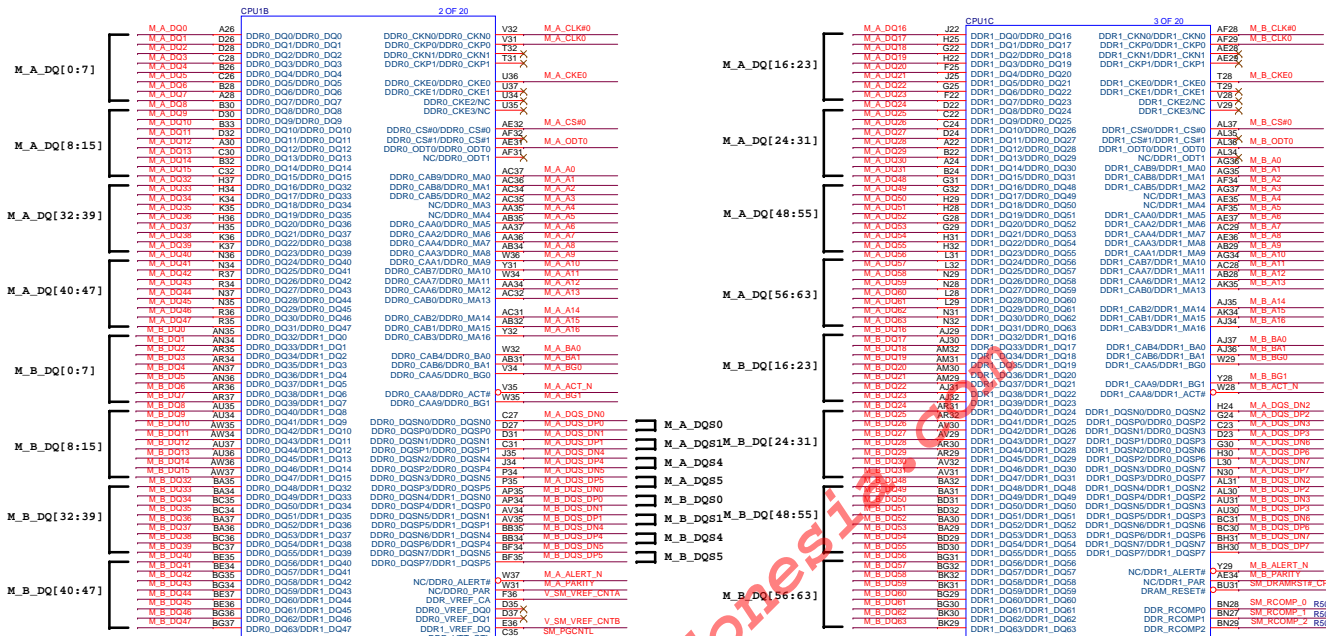
Date: Thursday, July 19, 2018 Sheet 4 of 106



SSID = CPU



## DDR4 ball type: Non-Interleaved Type



## 6.3.8 Coffee Lake U PDG x8 and x16 memory Down Routing Guidelines is Updated

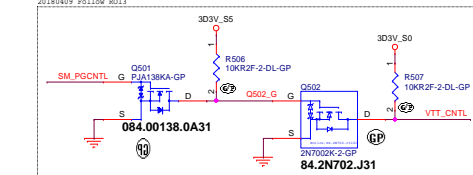
Coffee Lake U PDG (IBP #571021) x8 and x16 memory down routing guidelines has been updated.

Chapter 4.3.2 Table 4-12 CFL U DDR4 x16 Memory Down Routing Guidelines (mils):

- Rcomp [0] = 200/121
- Rcomp [1] = 80.6
- Rcomp [2] = 100

Chapter 4.3.3 Table 4-16 CFL U DDR4 x8 Memory Down Routing Guidelines (mils):

- Rcomp [0] = 121
- Rcomp [1] = 80.6
- Rcomp [2] = 100





[15] CFG3 << >> \_\_\_\_\_

[15] CFG4 << >> \_\_\_\_\_



[BDW Only]PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	
CFG[3]	0 : ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR
	1 : DISABLED

DISPLAY PORT PRESENCE STRAP	
CFG[4]	0 : ENABLED An external Display Port device is connected to the Embedded Display Port.
	1 : DISABLED (Default) No Physical Display Port attached to Embedded DisplayPort*. No connect for disable.

DELL

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***CPU (RESERVED)***

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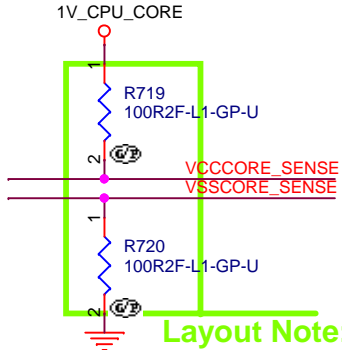
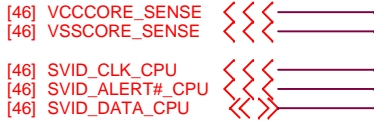
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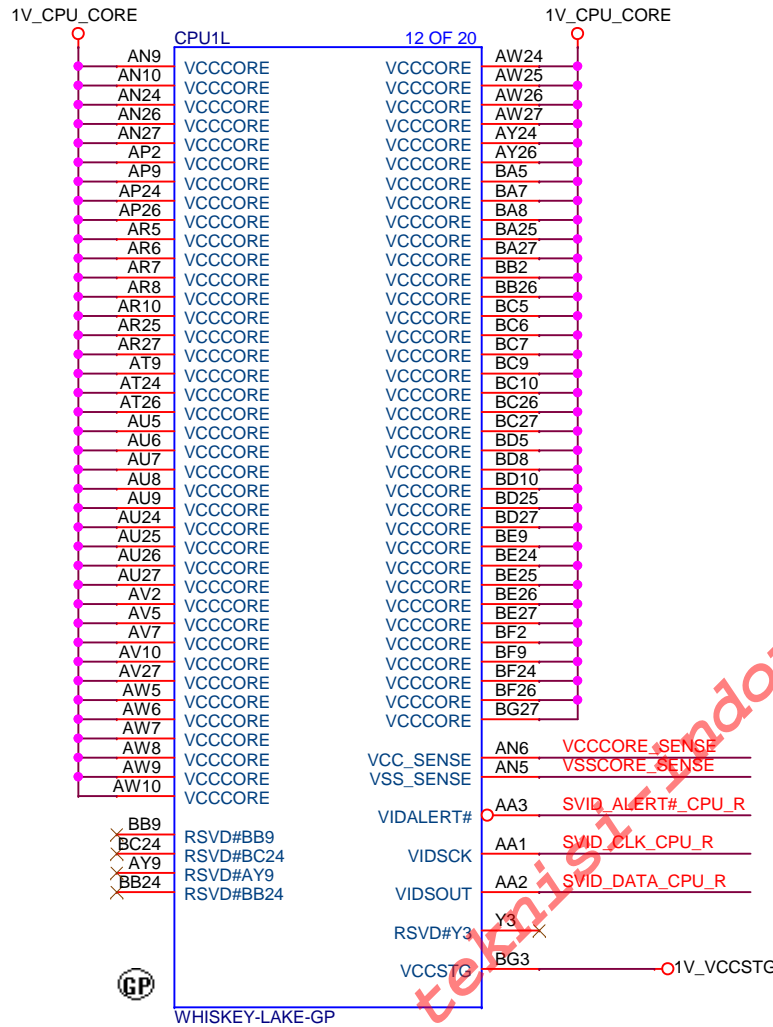
Sheet 6 of 106



**SSID = CPU**



- Layout Note:**
1. Place close to CPU
  2. VCC\_SENSE/ VSS\_SENSE impedance=50 ohm
  3. Length match<25mil



## SVID\_543016:

Layout Note:  
The total Length of Data and Clock (from CPU to each VR) must be equal ( $\pm 0.1$  inch).  
Route the Alert signal between the Clock and the Data signals.

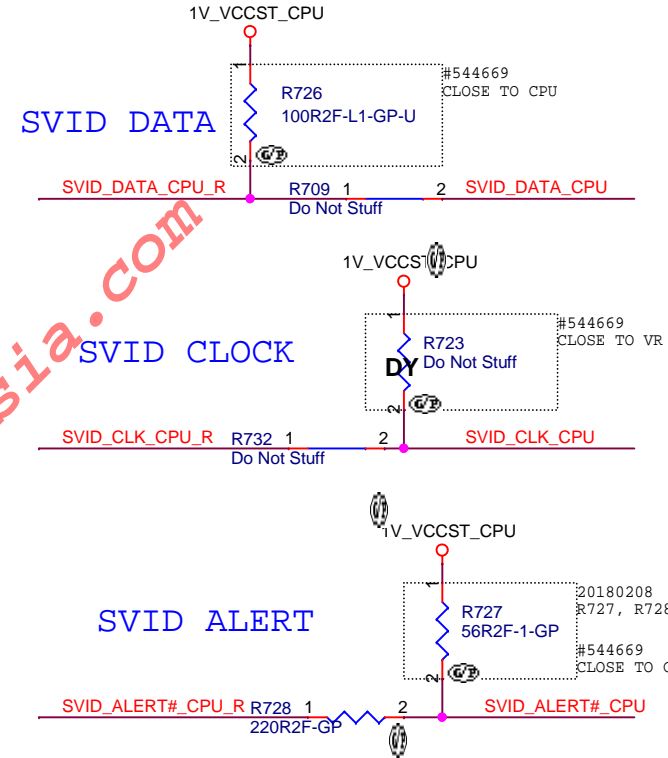
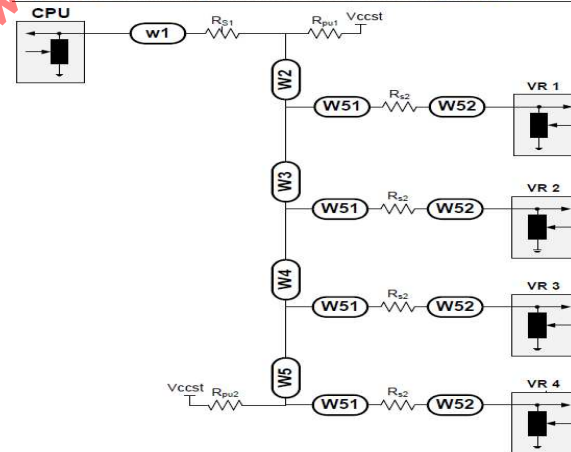


Figure 10-7. Routing Illustration for SVID Topology

Table 10-10. SVID Bus Routing Guidelines

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W51 [inches]	W52 [inches]	R <sub>pu1</sub> [Ω]	R <sub>pu2</sub> [Ω]	R <sub>s1</sub> [Ω]	R <sub>s2</sub> [Ω]	V <sub>CCST</sub> [V]
VIDSOUT	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	100	100	0	10	1.0
VIDSCK							Empty	45	0	50	
VIDALERT #							56	Empty	220	0	



<Core Design>



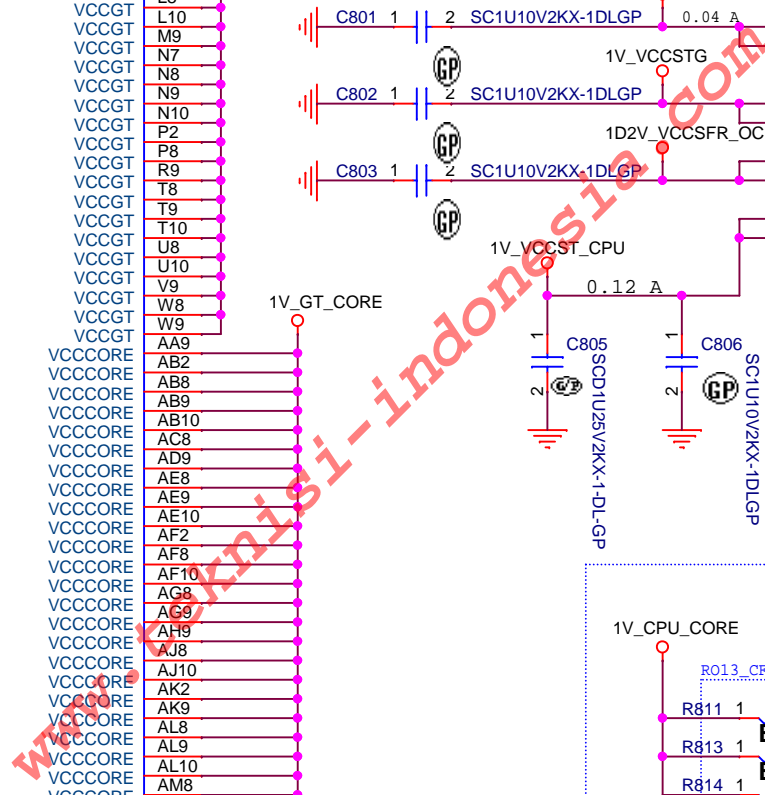
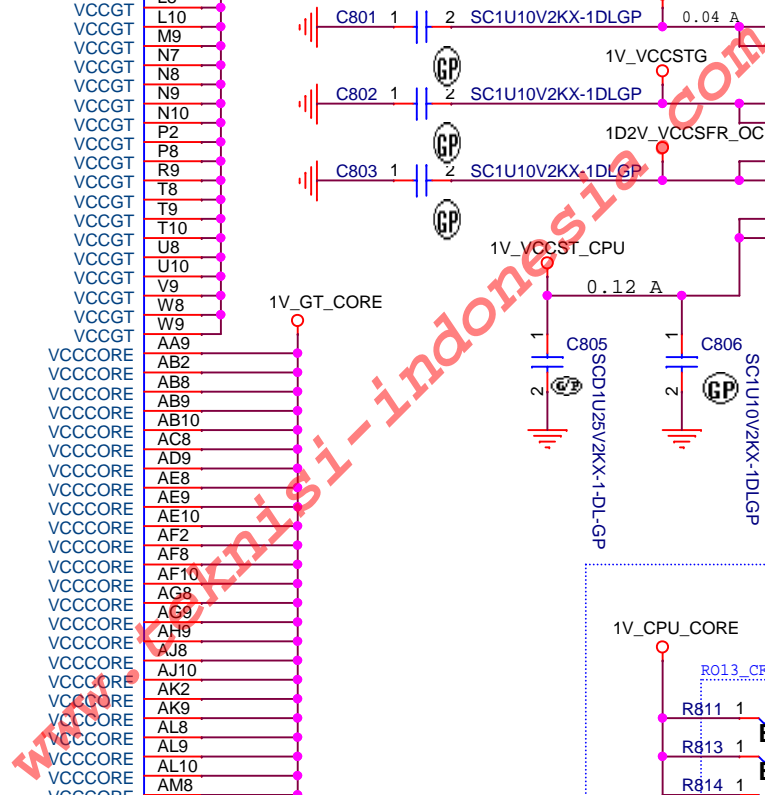
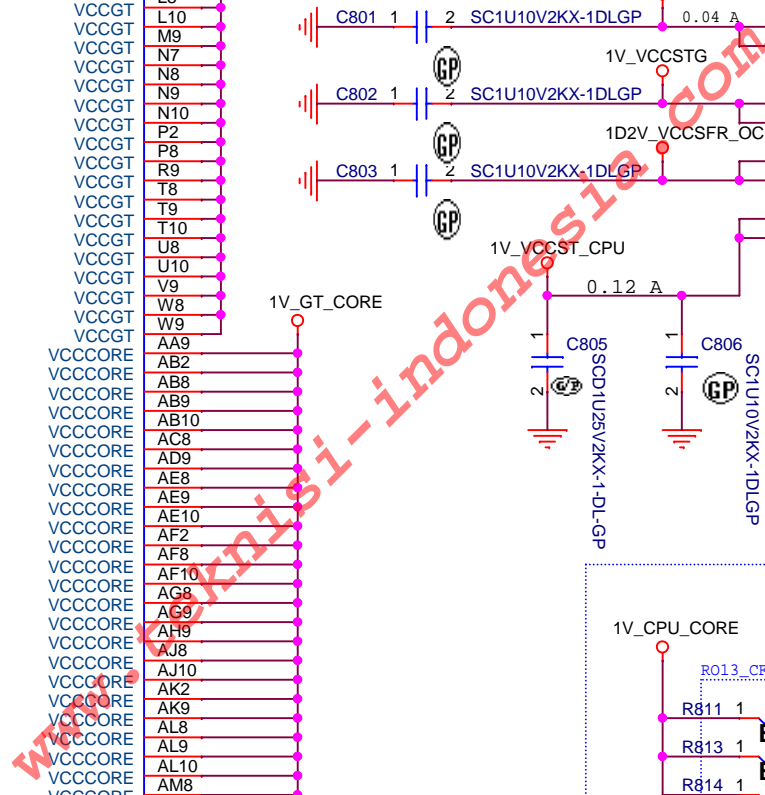
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Title <b>CPU(VCC CORE)</b>		
Size A4	Document Number <b>KR CS MLK 13"</b>	Rev <b>A00</b>
Date: Thursday, July 19, 2018	Sheet 7	of 106



[46] VCCGT\_SENSE <<< \_\_\_\_\_  
 [46] VSSGT\_SENSE <<< \_\_\_\_\_

[46] VSSSA\_SENSE <<< \_\_\_\_\_  
 [46] VCCSA\_SENSE <<< \_\_\_\_\_



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Title			
<b><i>CPU (DISPLAY)</i></b>			
Size A4	Document Number <b><i>KR CS MLK 13"</i></b>	Rev <b><i>A00</i></b>	
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**CPU (DISPLAY)**

**KR CS MLK 13"**

Sheet 8 of 106



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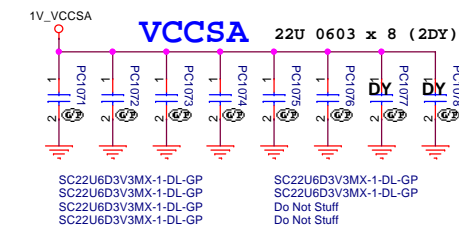
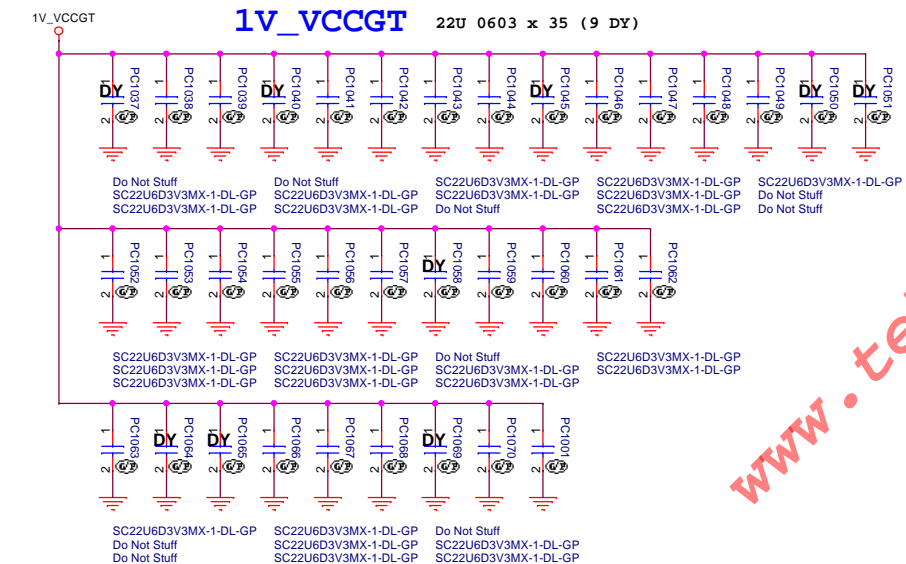
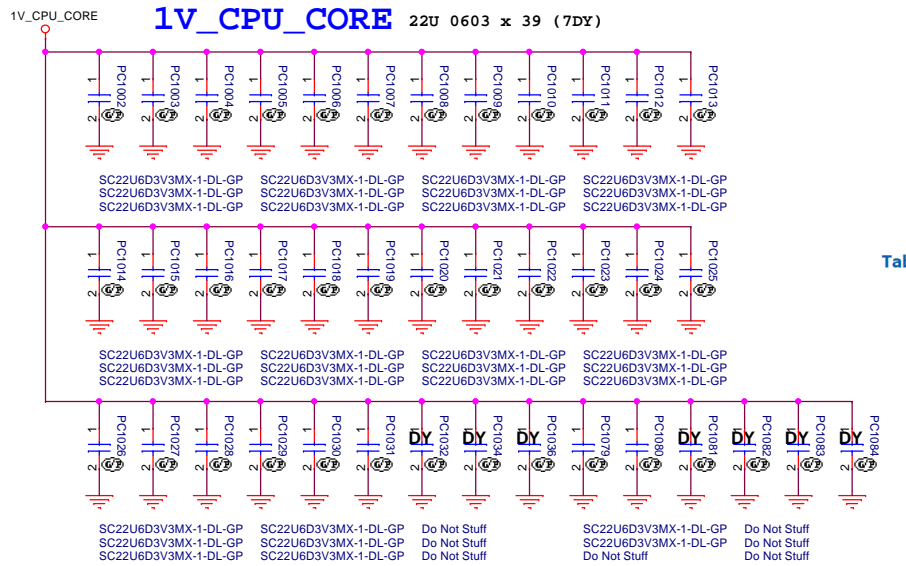
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Title <b>(Reserved)</b>			
Size A4	Document Number <b>KR CS MLK 13"</b>		Rev <b>A00</b>
Date: Thursday, July 19, 2018		Sheet 9	of 106



## SSID = CPU



**Table 11-5. Whiskey Lake U 4+2/Whiskey Lake U 4+2f/Cannon Lake U 2+2/ Coffee Lake U 4+3e Bulk Decoupling Example**

Bulk Decoupling Locations	Example WHL U42	Example WHL U42f	Example CNI U22	Example CFL U43e	Notes
VCC <sub>CORE</sub> Power Plane at VR output	4x 220uF (@4.5mΩ ESR)	3x 220uF (@4.5mΩ ESR)	TBD	3x 220uF (@4.5mΩ ESR)	Placed at primary side near to VR output
Vcc <sub>GT</sub> Power Plane at VR output	4x 220uF (@4.5mΩ ESR)	2x 220uF (@4.5mΩ ESR)	TBD	4x 220uF (@4.5mΩ ESR)	Placed at primary side near to VR output
<b>Notes:</b> 1. These examples are based on 1MHz switching frequency VR with bandwidth of up to 250KHz. 2. Bulk decoupling is not a "requirement" but recommendation only. It is an example of VR design/VR bandwidth. Customer should work with respective vendor to validate their VR & bulk decoupling design to ensure the electrical requirements are met.					

**Table 11-6. Decoupling Requirements for Whiskey Lake U 4+2/ Coffee Lake U 4+2f/ Cannon Lake U 2+2/ Coffee Lake U 4+3e Processor (Sheet 1 of 2)**

Domain	Primary Side cap	Secondary Side cap	Placement guideline
VCC <sub>CORE</sub>		35x 1uF 0402/0201	To be placed as close as possible to the vias that connected to the BGA pins.
		14x 10uF 0402	
		9x 22uF 0603	
	8x 10uF 0402		Place as close to the package as possible
	18x 47uF 0805 (6.3V)		Place as close to the package as possible. Can be placed on as either Primary or back side cap.
VCC <sub>CORE</sub> -VCC <sub>GT</sub> _ISLAND		7x 1uF 0402/0201	Place as close as possible to the package.
		7x 10uF 0402	

**Table 11-6. Decoupling Requirements for Whiskey Lake U 4+2/Coffee Lake U 4+2f/ Cannon Lake U 2+2/ Coffee Lake U 4+3e Processor (Sheet 2 of 2)**

Domain	Primary Side cap	Secondary Side cap	Placement guideline
VCC <sub>GT</sub>		11x 1uF 0402/0201	Place as close to the package as possible
		15x 10uF 0402	
	15x 22uF 0603		
	8x 47uF 0805 (6.3V)		
	7x 0603		Placeholder only
VCC <sub>SA</sub>	2x 0805		Placeholder only
		7x 1uF 0201	Place as close to the package as possible
		9x 10uF 0402	
	6x 10uF 0402		
	2x 47uF 0805 (6.3V)		
V <sub>DDQ</sub>	2x 0805		Placeholder Only
		4x 1uF 0402/0201	Place as close to the package as possible.
		3x 10uF 0402	
	1x 22uF 0603		
VCC <sub>SD</sub>	6x 10uF 0402		
	4x 1uF 0201		Place as close to the package as possible
		4x 1uF 0402/0201	Place as close to the package as possible
		6x 10uF 0402	
	4x 0402		Placeholder Only
VCC <sub>PLL_OC</sub>	1x 1uF 0402		Do not merge VCC <sub>PLL</sub> , VCC <sub>PLL_OC</sub> and VCC <sub>GT</sub> to any noisy and high current power rail and do not route them close adjacent to and reference to, any noisy and high current rail on top and bottom layers - as this may impact to PLL failing to phase lock.
VCC <sub>PLL</sub>	1x 0.1uF 0201		Place as close as possible to BGA.
	1x 1uF 0402		Place as close as possible to BGA and can be placed on either Primary or backside cap.
	1x 0805		Placeholder Only. Can be placed on as either Primary or back side cap.
VCC <sub>ST</sub>	1x 1uF 0402		
VCC <sub>STG</sub>	1x 1uF 0402		
VCC <sub>SDIO</sub>		6x 1uF 0201	Place as close to the package as possible.
		2x 22uF 0603	VCC <sub>SDIO</sub> and VCC <sub>SDIC</sub> rails are merged on board. VT to be placed as close as possible to BGA and a wide plane routing to meet DC_R <= 7mOhm.
VCC <sub>SDIC</sub>		4x 10uF 0402	VCC <sub>SDIO</sub> and VCC <sub>SDIC</sub> is required for CPL-U43e SKUs only
		2x 22uF 0603	

**Notes:**

1. The 6.3V voltage is for the higher capacitance retention; more 0805 components will be required for a lower voltage capacitor rating. Assumption: VR loop bandwidth ~ 250kHz e.g., 1MHz switching VR
2. Component placement order: Package edge > 0402 caps > 0603 caps > 0805 caps > Bulk caps > Power source.



Figure 11-11. Whiskey Lake U 4+2/Coffee Lake U 4+2f/Cannon Lake U 2+2/Coffee Lake U 4+3e Processor - RSHUNT Routing and Placement Guideline

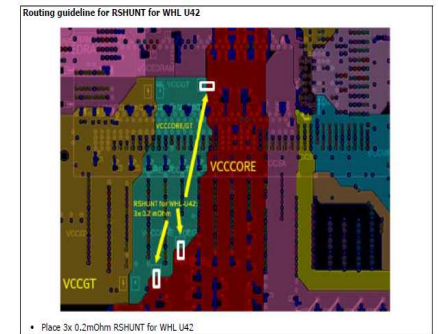
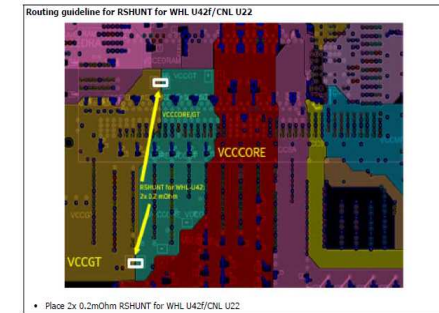


Figure 11-11. Whiskey Lake U 4+2/Coffee Lake U 4+2f/Cannon Lake U 2+2/Coffee Lake U 4+3e Processor - RSHUNT Routing and Placement Guideline



## <Core Design>



Title	<b>CPU (Power CAP1)</b>
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Size A3 Document Number **KR CS MLK 13"** Rev A0



Sheet 11 of 106



```

M_A.DQS_DNP[0] <<<
M_A.DQS_DNP0
M_A.DQS_DNP1
M_A.DQS_DNP2
M_A.DQS_DNP3
M_A.DQS_DNP4
M_A.DQS_DNP5
M_A.DQS_DNP6
M_A.DQS_DNP7

[M] M_A.DQS_DPP[0] <<<
M_A.DQS_DPP0
M_A.DQS_DPP1
M_A.DQS_DPP2
M_A.DQS_DPP3
M_A.DQS_DPP4
M_A.DQS_DPP5
M_A.DQS_DPP6
M_A.DQS_DPP7

[M] M_A.DQ0 <<<
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[M] M_A.DQ2 <<<
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[M] M_A.DQ27 <<<
[M] M_A.DQ28 <<<
[M] M_A.DQ29 <<<
[M] M_A.DQ30 <<<
[M] M_A.DQ31 <<<

[M] M_A.DQ32 <<<
[M] M_A.DQ33 <<<
[M] M_A.DQ34 <<<
[M] M_A.DQ35 <<<
[M] M_A.DQ36 <<<
[M] M_A.DQ37 <<<
[M] M_A.DQ38 <<<
[M] M_A.DQ39 <<<

[M] M_A.DQ40 <<<
[M] M_A.DQ41 <<<
[M] M_A.DQ42 <<<
[M] M_A.DQ43 <<<
[M] M_A.DQ44 <<<
[M] M_A.DQ45 <<<
[M] M_A.DQ46 <<<
[M] M_A.DQ47 <<<

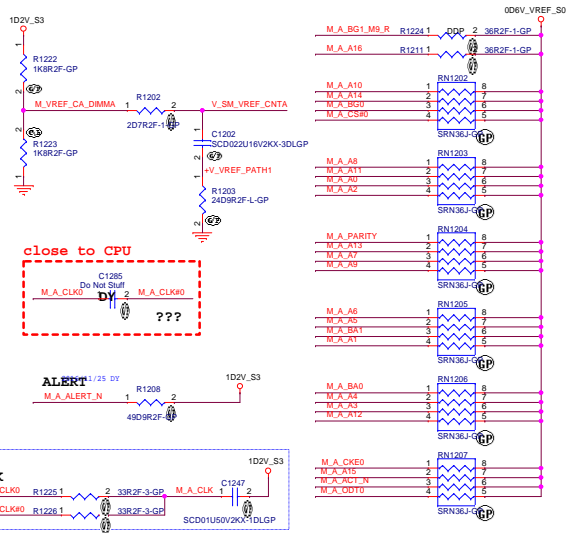
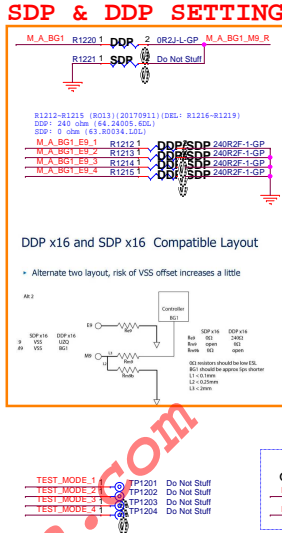
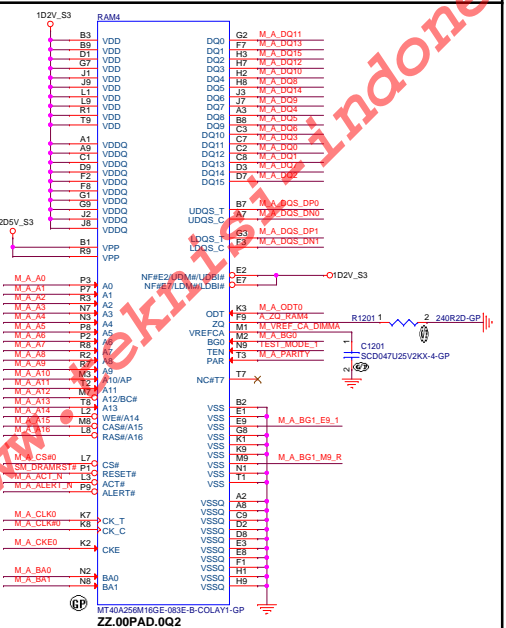
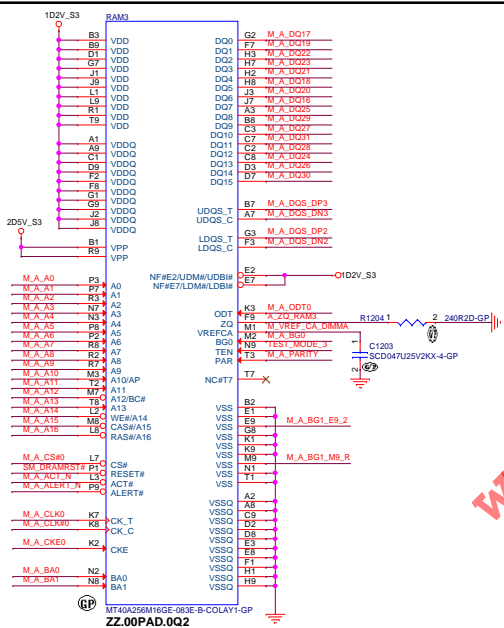
[M] M_A.DQ48 <<<
[M] M_A.DQ49 <<<
[M] M_A.DQ50 <<<
[M] M_A.DQ51 <<<
[M] M_A.DQ52 <<<
[M] M_A.DQ53 <<<
[M] M_A.DQ54 <<<
[M] M_A.DQ55 <<<

[M] M_A.DQ56 <<<
[M] M_A.DQ57 <<<
[M] M_A.DQ58 <<<
[M] M_A.DQ59 <<<
[M] M_A.DQ60 <<<
[M] M_A.DQ61 <<<
[M] M_A.DQ62 <<<
[M] M_A.DQ63 <<<

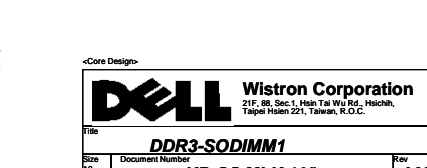
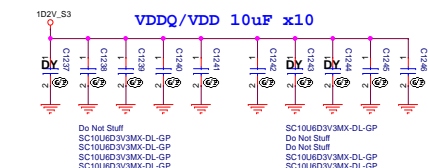
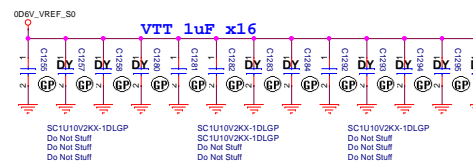
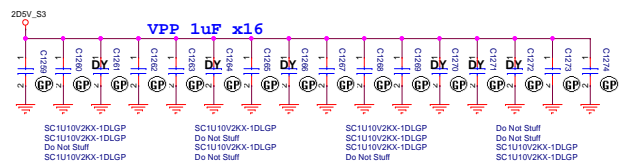
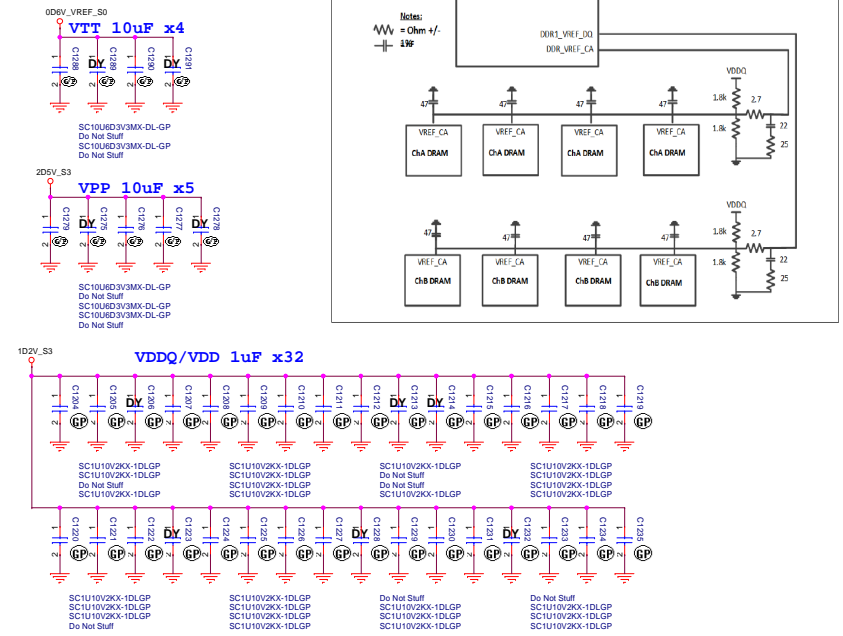
[M] M_A.A0 <<<
[M] M_A.A1 <<<
[M] M_A.A2 <<<
[M] M_A.A3 <<<
[M] M_A.A4 <<<
[M] M_A.A5 <<<
[M] M_A.A6 <<<
[M] M_A.A7 <<<
[M] M_A.A8 <<<
[M] M_A.A9 <<<
[M] M_A.A10 <<<
[M] M_A.A11 <<<
[M] M_A.A12 <<<
[M] M_A.A13 <<<
[M] M_A.A14 <<<
[M] M_A.A15 <<<
[M] M_A.A16 <<<

[M] V_SM.WREF_CNT[0] >>>
[M] M_A.00T0 >>>
[M] M_A.B00 >>>
[M] M_A.PARITY >>>
[M] M_A.CLK0 >>>
[M] M_A.CLK90 >>>
[M] M_A.CKE0 >>>
[M] M_A.CS#0 >>>
[M] SM.DRAMSTRB >>>
[M] M_A.ACT_N >>>
[M] M_A.ALERT_N >>>
[M] M_A.BA0 >>>
[M] M_A.BA1 >>>
[M] M_A.BG1 >>>

```



**Figure 4-8. WHL U DDR4 x16 Devices Memory Down V<sub>REF-CA</sub> Overview**





The diagram shows two groups of signals, **M\_B\_DQS\_DN[7:0]** and **M\_B\_DQS\_DP[7:0]**. Each group is associated with a red double arrow indicating a 10 ns period. The signals are labeled **M\_B\_DQS\_0** through **M\_B\_DQS\_7**.

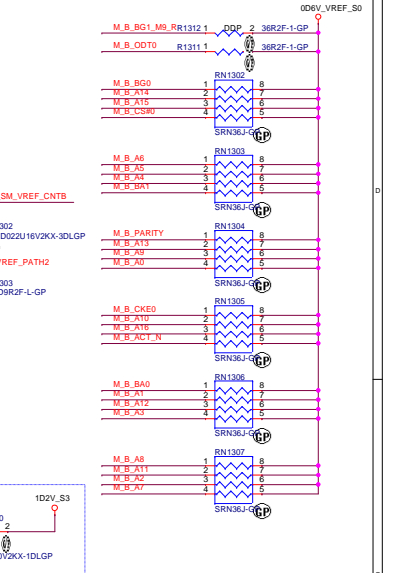
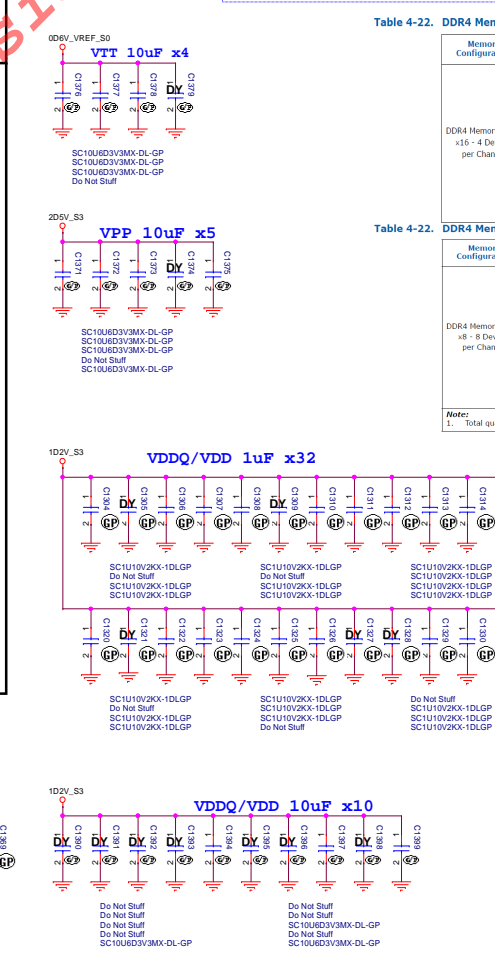
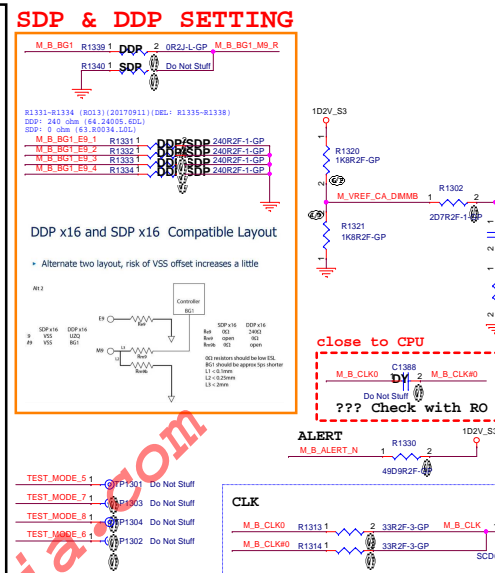
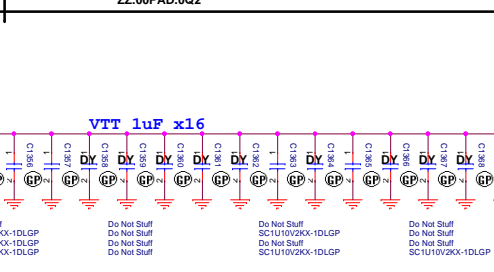
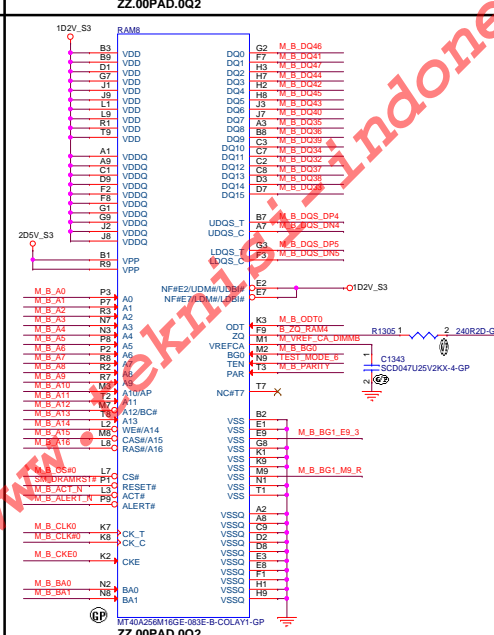
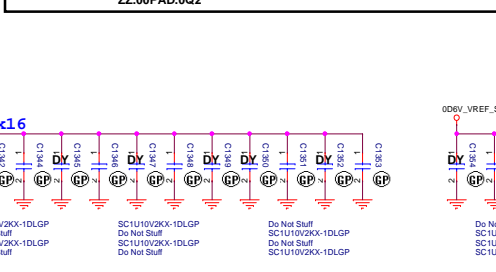
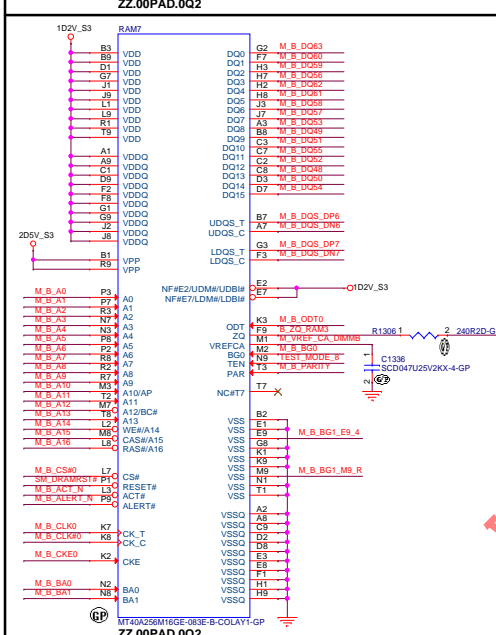
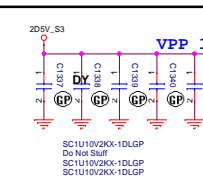
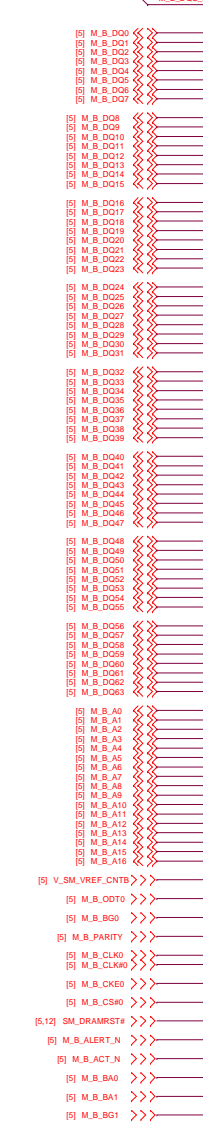


Table 4-22. DDR4 Memory Down Power Plane Decoupling (Sheet 1 of 2)

Memory Configuration	Power Domain	Decoupling Location	Qty x $\mu$ F (size)
DDR4 Memory Down x16 - 4 Devices per Channel	VDDQ/VDD (shorted)	4 per dram, as close as possible  distribute evenly across domain, close by Drams	32x 1 $\mu$ F (0402) (All stuffed)  10x 10 $\mu$ F (0603) (All stuffed)
	VPP	2 per dram, as close as possible  distribute evenly across domain, close by Drams	16x 1 $\mu$ F (0402)  5x 10 $\mu$ F (0603)
	VTT	distributed along termination resistors	16x 1 $\mu$ F (0402)
		distribute evenly across	1x 10 $\mu$ F (0603)

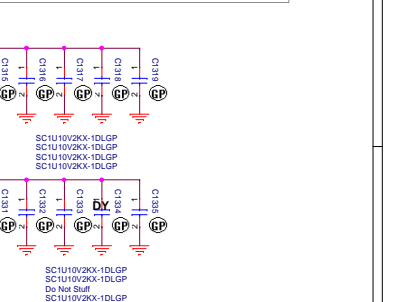
		domain	4x 10µF (0003)
--	--	--------	----------------

**Table 4-22. DDR4 Memory Down Power Plane Decoupling (Sheet 2 of 2)**

Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)
DDR4 Memory Down x8 - 8 Devices per Channel	VDDQ/VDD (shorted)	4 per dram, as close as possible	64x 1µF (0402) (min of 48 stuffed)
		distribute evenly across domain, close by Drams	20x 1µF (0603) (min of 12 stuffed)
	VPP	2 per dram, as close as possible	32x 1µF (0402)
		distribute evenly across domain, close by Drams	10x 10µF (0603)
		distributed along termination resistors	32x 1µF (0402)
	VTT	distribute evenly across domain	8x 10µF (0603)

**Note:**

1. Total quantity is referring to 2 channels.





(Blanking)

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<Core Design>

			<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title <b>(Reserved)_SODIMM _SODIMM4</b>					
Size A4		Document Number <b>KR CS MLK 13"</b>			Rev <b>A00</b>
Date: Thursday, July 19, 2018		Sheet 14 of 106			



0x12000000	0x12000000	0x12000000
0x12000001	0x12000001	0x12000001
0x12000002	0x12000002	0x12000002
0x12000003	0x12000003	0x12000003
0x12000004	0x12000004	0x12000004
0x12000005	0x12000005	0x12000005
0x12000006	0x12000006	0x12000006
0x12000007	0x12000007	0x12000007
0x12000008	0x12000008	0x12000008
0x12000009	0x12000009	0x12000009
0x1200000A	0x1200000A	0x1200000A
0x1200000B	0x1200000B	0x1200000B
0x1200000C	0x1200000C	0x1200000C
0x1200000D	0x1200000D	0x1200000D
0x1200000E	0x1200000E	0x1200000E
0x1200000F	0x1200000F	0x1200000F
0x12000010	0x12000010	0x12000010
0x12000011	0x12000011	0x12000011
0x12000012	0x12000012	0x12000012
0x12000013	0x12000013	0x12000013
0x12000014	0x12000014	0x12000014
0x12000015	0x12000015	0x12000015
0x12000016	0x12000016	0x12000016
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0x12000018	0x12000018	0x12000018
0x12000019	0x12000019	0x12000019
0x1200001A	0x1200001A	0x1200001A
0x1200001B	0x1200001B	0x1200001B
0x1200001C	0x1200001C	0x1200001C
0x1200001D	0x1200001D	0x1200001D
0x1200001E	0x1200001E	0x1200001E
0x1200001F	0x1200001F	0x1200001F

GPP_B14 / SPMR	The Shared Channel	Rising edge of PCH_PWROK
----------------	--------------------	--------------------------



GPP_B18 / GSPID_MOSI	No Reboot	Rising edge of PCH_PWROK
----------------------	-----------	--------------------------



GPP_C2 / SMBALERT#	TLS Confidentiality	Rising edge of RSMRST#
--------------------	---------------------	------------------------



GPP_C2 / SMBALERT#	Flash BIOS/BIOS Setup	Rising edge of PCH_PWROK
--------------------	-----------------------	--------------------------



GPP_C5 / SMBALERT#	eSPI or LPC	Rising edge of RSMRST#
--------------------	-------------	------------------------



SPID_MOSI	Reserved	Rising edge of RSMRST#
-----------	----------	------------------------



GPP_D12 / ISH_SPI_MOSI / GSPID_MOSI	Reserved	Rising edge of RSMRST#
-------------------------------------	----------	------------------------



GPP_B23 / SMBALERT# / PCHHOT#	Intel® DCI+O0B	Rising edge of RSMRST#
-------------------------------	----------------	------------------------



SPID_I02	Reserved	Rising edge of RSMRST#
----------	----------	------------------------



SPID_I03	Reserved	Rising edge of RSMRST#
----------	----------	------------------------



HDA_SDO / I2SD_TXD	Flash Descriptor Security Override	Rising edge of PCH_PWROK
--------------------	------------------------------------	--------------------------



GPP_E19 / DDPB_CTRLDATA / CNV_BT_IF_SELECT	Display Port B Detected	Rising edge of PCH_PWROK
--	-------------------------	--------------------------



GPP_E21 / DDPB_CTRLDATA	Display Port C Detected	Rising edge of PCH_PWROK
-------------------------	-------------------------	--------------------------



GPP_E23 / DDPB_CTRLDATA	Display Port D Detected	Rising edge of PCH_PWROK
-------------------------	-------------------------	--------------------------



GPP_H17	Reserved	Rising edge of PCH_PWROK
---------	----------	--------------------------



GPP_H21	XTAL Frequency Select	Rising edge of RSMRST#
---------	-----------------------	------------------------



GPP_F6 / CNV_RGL_DT	M2 CNV Mode Select	Rising edge of RSMRST#
---------------------	--------------------	------------------------



INPUT3VSEL	3.0V Select	Input pin must always be driven to a valid logic level
------------	-------------	--



GPD7	Reserved	Rising edge of DSN_PWROK
------	----------	--------------------------



GPP_H23	eSPI Flash Sharing Mode	Rising edge of RSMRST#
---------	-------------------------	------------------------



[Show Only] PHYSICAL_DEVICE_ENABLED (SFX PRIVACY)	
SPID[3]	S - Disabled Not SFX Enabled bit in device interface MIB S - Disabled



(004014)	
DISPLAY PORT PRESENCE STRAP	
CPID[4]	0 = Disabled In external display Port device is connected to the Disabled Display Port. 1 = Enabled In external display Port device is connected to the Enabled Display Port.



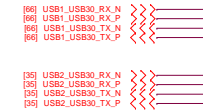


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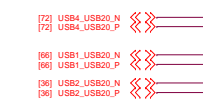
#543016:  
220 nF nominal capacitors are recommended for Gen 3.  
100 nF nominal capacitors are recommended for Gen 2.

(#545659) The xHCI controller supports USB Debug port on all USB3.0 capable ports.

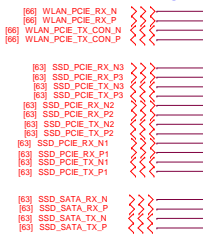
USB3.0



USB2.0



PCIe



PCIe



PCIe



PCIe



PCIe

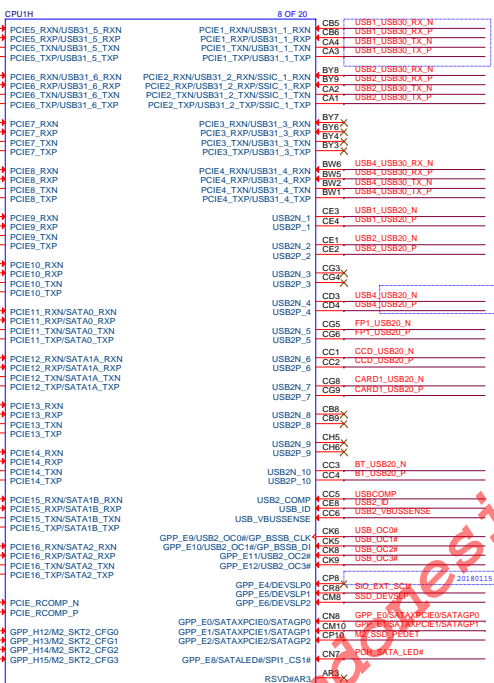


OPTANE MEMORY

SSD

Figure 6-1. High Speed I/O (HSIO) Lane Multiplexing in CNL U PCH-LP

Flex I/O Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
High Speed I/O (HSIO) Type and Lane	USB3.1 Gen1/Gen2 #1	USB3.1 Gen1/Gen2 #2	USB3.1 Gen1/Gen2 #3	USB3.1 Gen1/Gen2 #4	USB3.1 Gen1/Gen2 #5	USB3.1 Gen1/Gen2 #6	PCIe #7	PCIe #8	PCIe #9	PCIe #10	PCIe #11	PCIe #12	PCIe #13	PCIe #14	PCIe #15	PCIe #16
Intel® RST Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support



Layout Note:

- 1. Trace Width: 4 mils min (breakout) 12-15 mils (trace)
- Note: Must maintain low DC resistance routing (<0.1 ohm).
- 2. Isolation Spacing: At least 12 mils to any adjacent high speed I/O.

(#543016) Unused SATA/GP[2:0] GPP[21:0] pins must be terminated to either 3.3 V rail or GND using 8.2 KΩ to 10 KΩ on the motherboard. Do not use both pull-up and pull-down. Either pull-up or pull-down is acceptable.

USB 2.0 Table

Pair	Device
1	USB3.0 port1
2	N/A
3	USB3.0 Port2 (IOBD)
4	Type-c
5	CAMERA
6	WLAN
7	Touch Panel
8	Card Reader

#545659 (SKL\_PCH\_U\_Y\_EDS Rev0.7)

IO board USB3.0

RO13, 20170811 follow HSIO MAP

USB3.0 Type C

IO board USB3.0

MB USB3.0

USB3.0 Type C

Fingerprint Reader

CAMERA

Card Reader

WLAN (BT)

TYPEC

TYPEC

TYPEC

TYPEC

TYPEC

TYPEC

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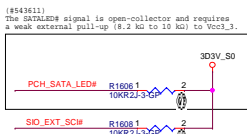
TYPEC

TYPEC

TYPEC

TYPEC

TYPEC



(#543016) When used as DEVLP, no external pull-up or pull-down termination required from SATA Host DEVLP.

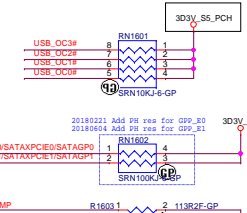


Table 24-3. PCI Express\* Link Configurations Supported

SKL	PCIe Link Config	PCI Express* Lanes											
		1	2	3	4	5	6	7	8	9	10	11	12
U	1x4	Port1				Port5				Port9			
	2x2	Port1	Port3			Port5			Port7			Port9	
	1x2 + 2x1	Port1	Port3	Port4	Port5	Port6	Port7	Port8	Port9		Port11	Port12	
	4x1	Port1	Port2	Port3	Port4	Port5	Port6	Port7	Port8	Port9	Port10	Port11	Port12
Y	1x4	Port1				Port5							
	2x2	Port1	Port3			Port5			Port7				
	1x2 + 2x1	Port1	Port3	Port4	Port5	Port6	Port7	Port8					
	4x1	Port1	Port2	Port3	Port4	Port5	Port6	Port7	Port8				
	1x2								Port9				
	2x1								Port9		Port10		

Table 24-2. PCI Express\* Port Feature Details

SKL	Max Device (Ports)	Max Lanes	PCIe* Gen Type	Encoding	Transfer Rate (MT/s)	Theoretical Max Bandwidth (GB/s)
U	6	12	1	8b/10b	2500	0.25
			2	8b/10b	5000	0.50
			3	128b/130b	8000	1.00
Y	5	10	1	8b/10b	2500	0.25
			2	8b/10b	5000	0.50

<Core Design>

**Wistron Corporation**  
21F, 8B, Sec. 1, Hsin Tai Wu Rd., Hsueh-shan, Taipei Hsien 221, Taiwan, R.O.C.

File: **CPU (PCIe/SATA/USB)**

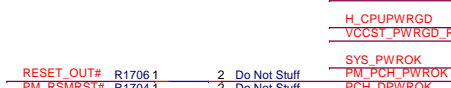
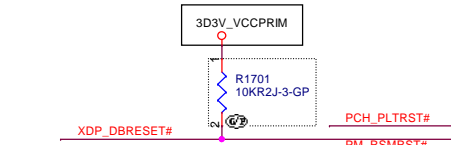
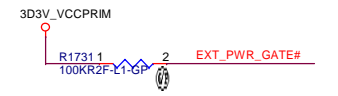
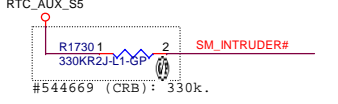
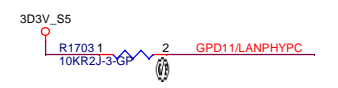
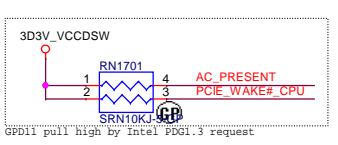
Size: **A2** | Document Number: **KR CS MLK 13"** | Rev: **A00**

Date: **Thursday, July 19, 2018** | Sheet: **16** of **106**

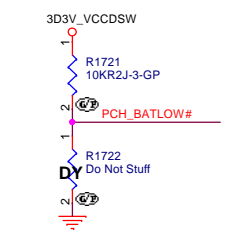
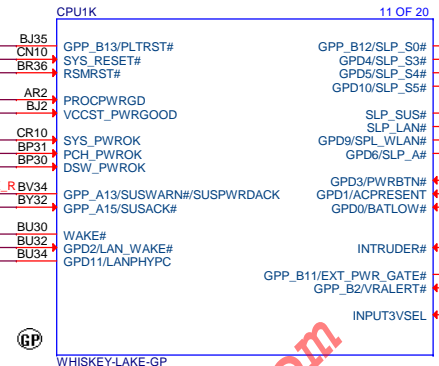


SSID = PCH

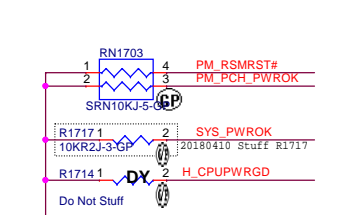
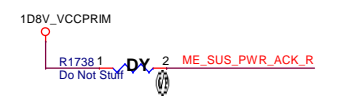
- [24] SYS\_PWROK >>>
- [24.26] RESET\_OUT# >>>
- [24.40] VCCST\_PWRGD >>>
- [24] PCH\_RSMRST# >>>
- [25,40,45] 3V\_5V\_PWRGD >>>
- [40,91] PM\_SLP\_S0# <<<
- [40,51] PM\_SLP\_S3# <<<
- [40,53] PM\_SLP\_S4# <<<
- [24,61] AUX\_EN\_WOVL <<<
- [24] SIO\_PWRBTN# >>>
- [43,44] AC\_IN# >>>
- [26,63,66,91] PLTRST#\_CPU <<<
- [3] H\_CPUPWRGD <<<
- [15] INPUT3VSEL >>>



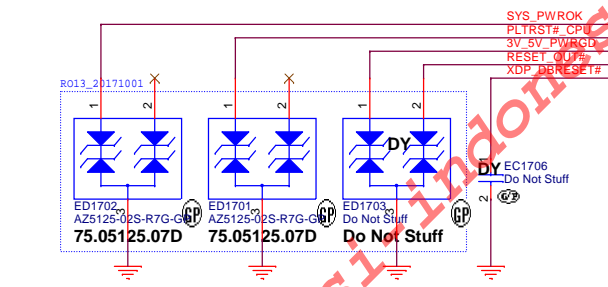
[#543016 Rev0.7]  
EXT\_PWR\_GATE#: Due to a bug on A0,  
a temporary pull-up resistor will be required to overcome  
the internal 20k pull-down  
that is active during the early portion of the power up sequence



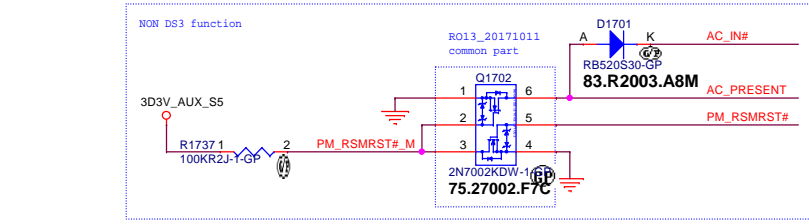
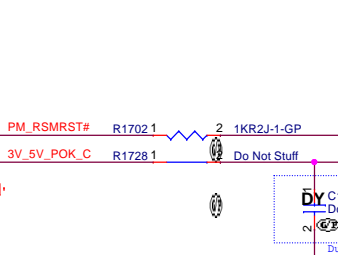
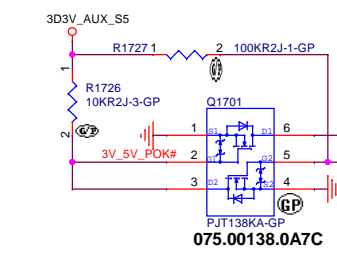
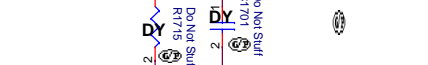
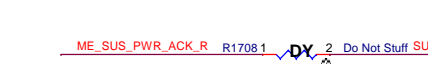
RO13\_20171027 PCH\_BATLOW#  
Software set GPD0 avoid PCH屬性BATLOW# PU會漏電  
不接R1704.6 PU是因為Layout走不過去



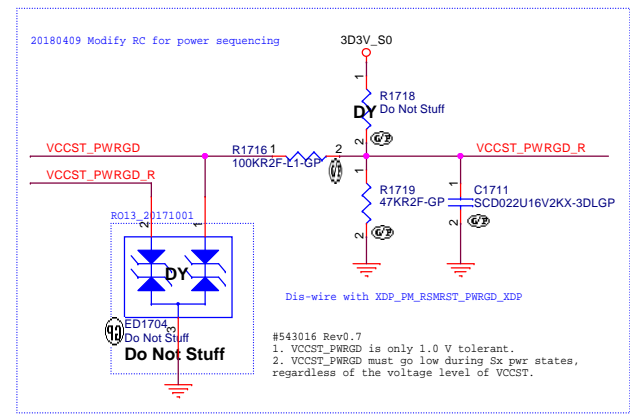
A02 Power switch, P/N: 074.01334.0093  
Low Rds(on) = 5m Ohm  
Turn on rise time = 10us  
#544669 Rev0.52 CRB:  
No PL resistor on THERMTRIP#.



BATLOW#:  
Pull-up required even if not implemented.  
RO13\_20171027 PCH\_BATLOW#  
Software set GPD0 avoid 屬性BATLOW# PU會漏電



Power Sequence



#543016 Rev0.7  
1. VCCST\_PWRGD is only 1.0 V tolerant.  
2. VCCST\_PWRGD must go low during Sx pwr states,  
regardless of the voltage level of VCCST.

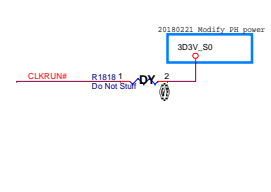
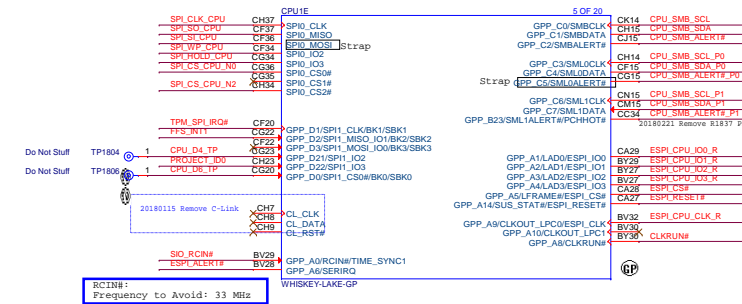
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**CPU\_(POWER MANAGEMENT)**

Size A3 Document Number KR CS MLK 13" Rev A00  
Date: Thursday, July 19, 2018 Sheet 17 of 106



[60]	WLAN_CLK_CPU_N	<<>	
[60]	WLAN_CLK_CPU_P	<<>	
[66]	WLAN_CLKREQ_CPU_P	<<>	
[83]	SSD_CLK_CPU_N	<<>	
[63]	SSD_CLK_CPU_P	<<>	
[63]	SSD_CLKREQ_CPU_N	<<>	
[25,91]	SPI_SIO_CPU	>>>	
[25,91]	SPI_CLK_CPU	>>>	
[15,25,91]	SPI_CS_CPU	>>>	
[91]	SPI_CS_CPU_N0	>>>	
[91]	SPI_CS_CPU_N2	>>>	
[15,25]	SPI_HOLD_CPU	<<<	
[15,25]	SPI_WP_CPU	<<<	
[24,68]	ESPI_CPU_ID[0..3]	<<<	ESPI_CPU_ID0 ESPI_CPU_ID1 ESPI_CPU_ID2 ESPI_CPU_ID3
[24,26]	CPU_SMB_SCL_P1	<<<	
[24,26]	CPU_SMB_SDA_P1	<<<	
[24,68]	ESPI_CS#	<<<	
[24,68]	ESPI_RESET#	<<<	
[24,68]	ESPI_CS#	<<<	
[24]	SUS_CLK	<<<	
[91]	TPM_SPI_IRQ#	>>>	
[24,25]	RTRCST_ON	>>>	
[15]	CPU_SMB_ALERT#	>>>	
[15]	CPU_SMB_ALERT#_P0	>>>	
[15]	CPU_SMB_ALERT#_P1	>>>	
[21]	PROJECT_ID0	>>>	
[70]	FFS_INT1	>>>	

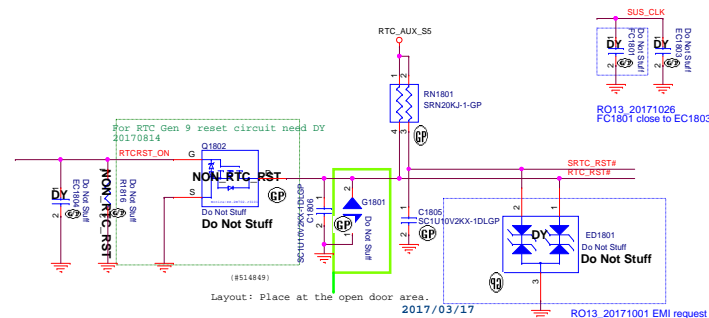
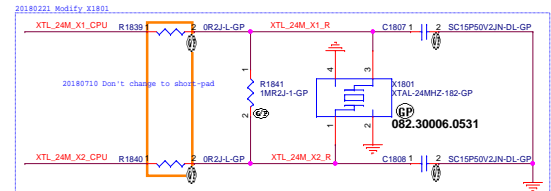
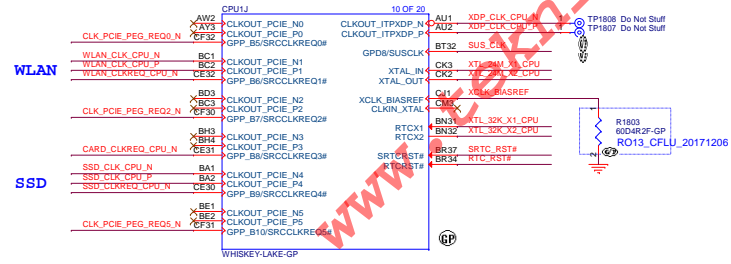
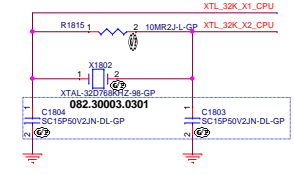


<b>BOOT HALT</b>	
<b>SPI0_MOSI</b>	0 = ENABLED 1 = DISABLED WEAK INTERNAL PU

This signal has a weak internal pull-up.

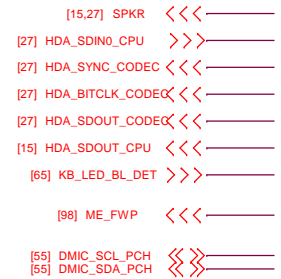
Table 3-1: Platform Supported Pin Strap Settings for LPC / eSPI / SPI Flash			
ESPI Enable Strap (ESPI_EN) Value (0: LPC, 1: eSPI)	Boot BIOS Strap (BBS) Value (0: SPI, 1: LPC/eSPI)	EC Connection	Boot (BIOS) Flash Connection (Section 3.1.4)
0	0	LPC	SPI
0	1	LPC	LPC
1	0	eSPI	SPI
1	1	eSPI	eSPI (to EC over eSPI Peripheral Channel) (refer to Section 3.1.4 for details)

Signal	Usage	When Sampled	Comment				
			<p>This signal has a weak internal Pull-down.</p> <p>This field determines the destination of accesses to the BIOS memory ranges. Also controllable using Boot BIOS Destination bit (BusD, Devnc13, Function), offset BCh, bit 6).</p>				
OSPI_HOST0/ GPB_022	Boot BIOS Strap Bit 8B5	Rising edge of PCH_PVWRC	<div><div><div>Bit 6</div><div>Boot BIOS Destination</div><table><tr><td>0</td><td>SPI (Default)</td></tr><tr><td>1</td><td>LPC</td></tr></table></div><div><p><b>Notes:</b></p><ol style="list-style-type: none"><li>The internal Pull-down is disabled after PLTRST# de-asserts.</li><li>If option 1 (LPC) is selected, BIOS may still be placed on LPC, but all platforms are required to have SPI flash connected directly to the PCSPi bus with a valid descriptor in order to boot.</li><li>Boot BIOS Destination select to LPC by functional strap or using Boot BIOS Destination bit will not assert SPI accesses initiated by Intel ME or Integrated OLE LAN.</li><li>This signal is in the primary well.</li></ol><p>This signal has a weak internal Pull-down.</p><p>0 = <b>LPC</b> is selected for EC. (Default) 1 = <b>eSPI</b> is selected for EC.</p><p><b>Notes:</b></p><ol style="list-style-type: none"><li>The internal Pull-down is disabled after RSMRST# de-asserts.</li><li>This signal is in the primary well.</li></ol></div></div>	0	SPI (Default)	1	LPC
0	SPI (Default)						
1	LPC						
SMIOALERT#/ GPB_CS	eSPI or LPC	Rising edge of RSMRST#					





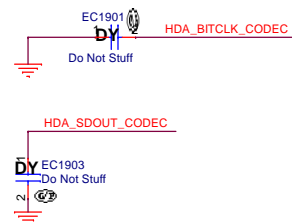
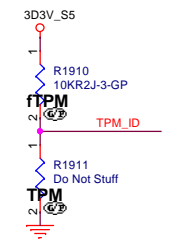
SSID = PCH



Strap pin:

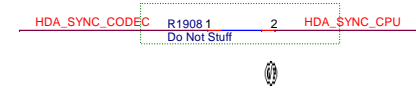
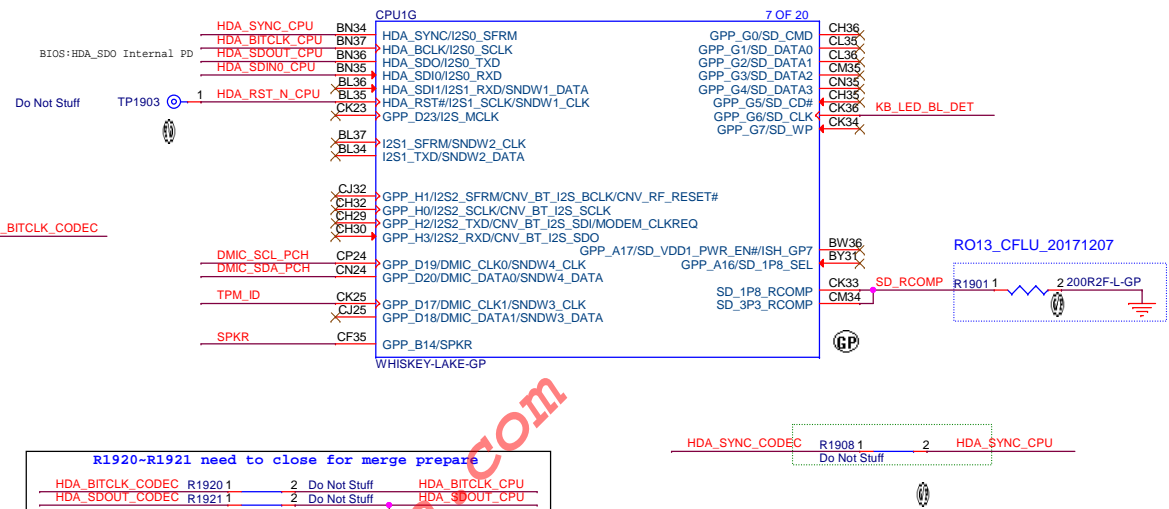
Port B / Port C Detected	Sampled at rising edge of PCH_PWROK
DDPB_CTRLDATA	0 = Port B is not detected. ★ 1 = Port B is detected.
DDPC_CTRLDATA	0 = Port C is not detected. ★ 1 = Port C is detected.

These two signals have weak internal pull-down.



RO13\_20171027  
delete ED1901

R1920-R1921 need to close for merge prepare					
HDA_BITCLK_CODECD	R1920 1	2	Do Not Stuff	HDA_BITCLK_CPU	
HDA_SDOUT_CODECD	R1921 1	2	Do Not Stuff	HDA_SDOUT_CPU	
ME_FWP	R1909 1				



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```

[55] CPU_I2C_SDA_P1 >>>
[55] CPU_I2C_SCL_P1 >>>

[65] CPU_I2C_SDA_P0 >>>
[65] CPU_I2C_SCL_P0 >>>

[55,70] CPU_I2C_SDA_ISH >>>
[55,70] CPU_I2C_SCL_ISH >>>

[68] UART_2_CRXD_DTXD >>>
[68] UART_2_CTXD_DRXD >>>

[55] GYRO_INT_C >>>
[55] GYRO_DRDY >>>

[70] GSEN2_INT1_C >>>
[70] GSEN2_INT2_C >>>
[70] FFS_INT2 >>>

[55] GSEN_INT1 >>>
[55] GSEN_INT2 >>>

[15] NRB_BIT >>>

[15,25] RTC_DET# >>>

[21] BOARD_ID2 >>>

[15] CNV_RGL_DT >>>

[65] KB_DET# >>>

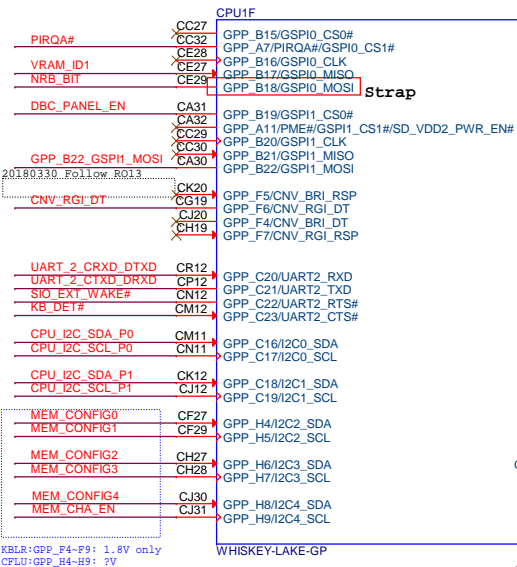
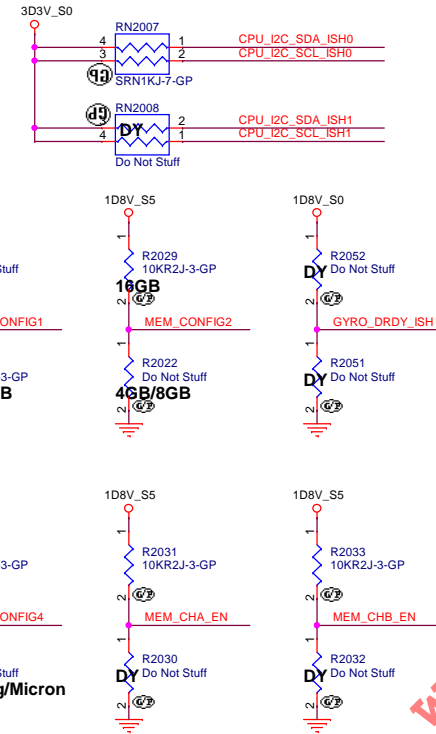
[24] SIO_EXT_WAKE# >>>

[15] GPP_B22_GSP11_MOSI >>>

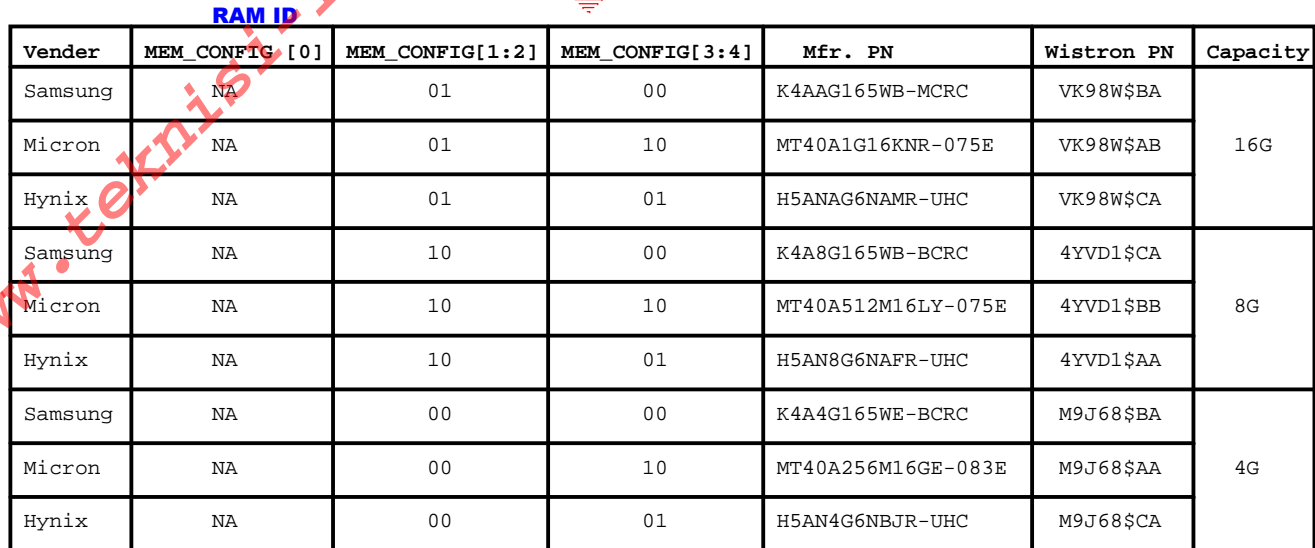
[91] PIRQA# <<<

[55] DBC_PANEL_EN <<<
[55] IR_CAM_DET# <<<
[24] NB_MODE# <<<

```



(PDG#543016) If the UART/GPIO functionality is also not used, the signals can be left as no-connect.



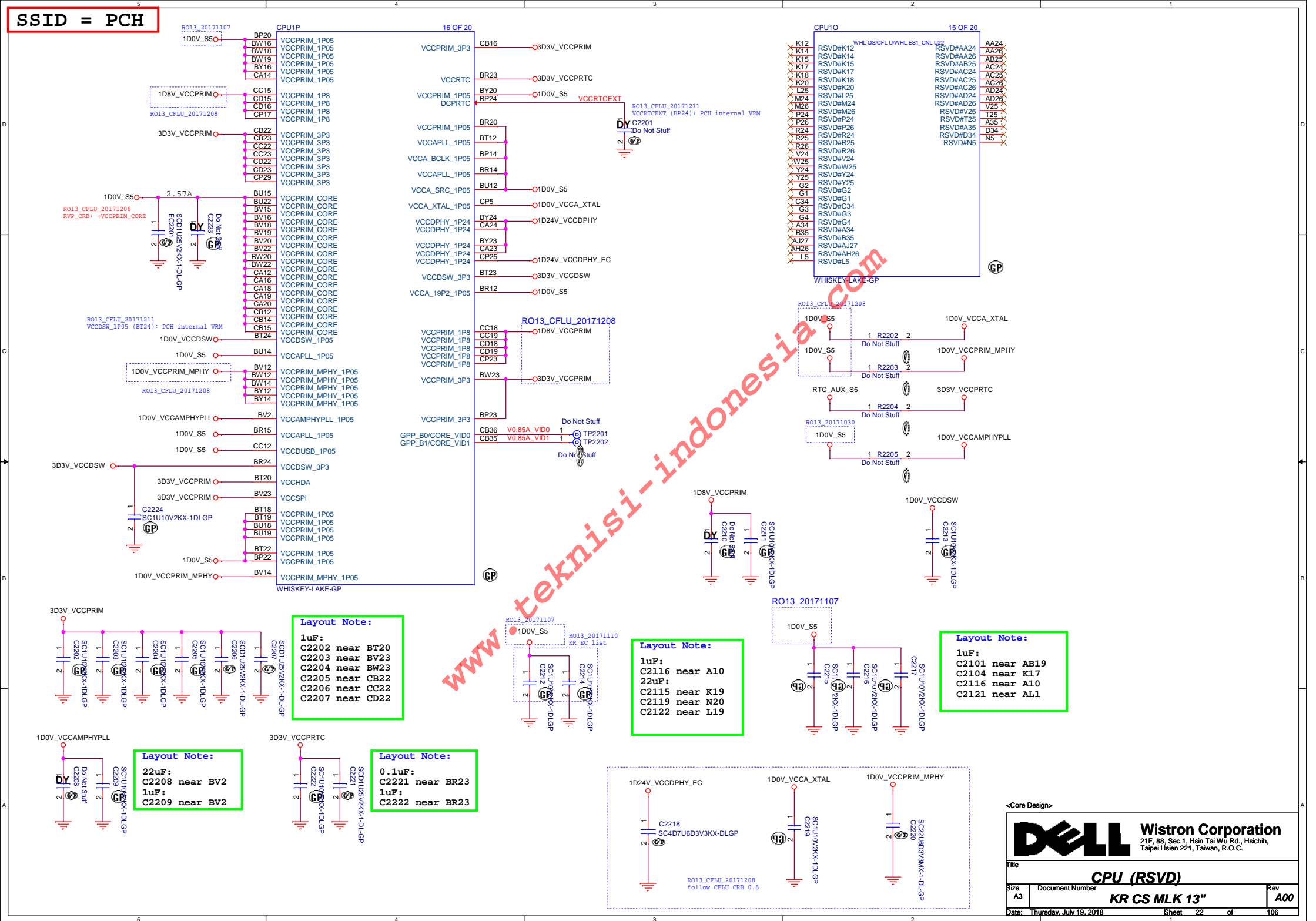
VRAM_ID[2:1]	dGPU VRAM size	11	UAM Board
		10	N/A
		01	DIS Board with 4GB VRAM
		00	DIS Board with 2GB VRAM



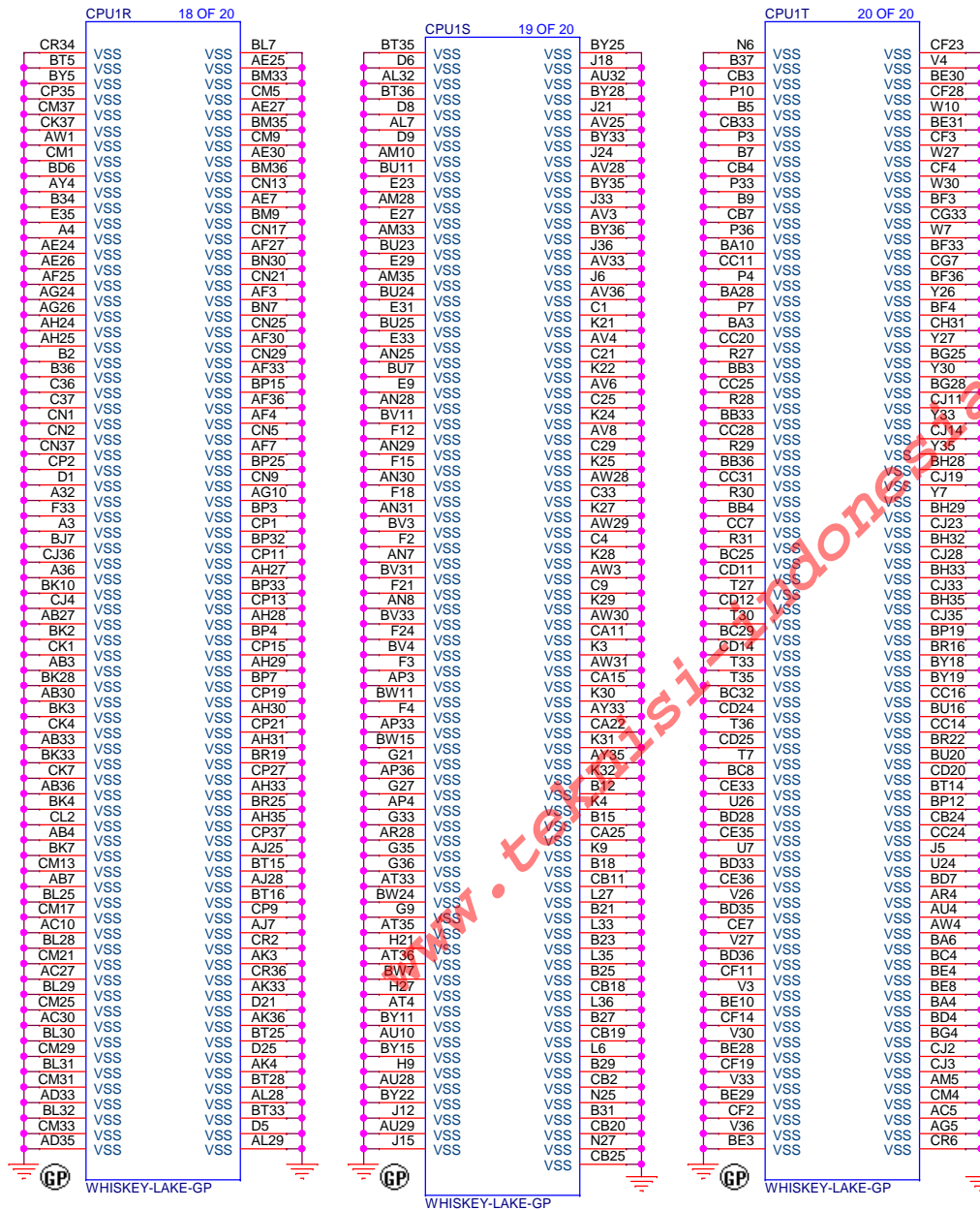




**SSID = PCH**







Skylake U Processor Corner NCTF Motherboard Test Point Example

Pin Number	Pin Name	Description	Corner
BB70	NCTFVSS	Test Point (TP)	Corner BB71
BB67	NCTFVSS	Test Point (TP)	
BA71	NCTFVSS	Test Point (TP)	
AV71	NCTFVSS	Test Point (TP)	
BA1	NCTFVSS	Test Point (TP)	Corner BB1
BA2	NCTFVSS	Test Point (TP)	
AV1	NCTFVSS	Test Point (TP)	Corner A1
C1	NCTFVSS	Test Point (TP)	
A5	NCTFVSS	Test Point (TP)	Corner A71
A70	NCTFVSS	Test Point (TP)	
A67	NCTFVSS	Test Point (TP)	
B71	NCTFVSS	Test Point (TP)	
E71	NCTFVSS	Test Point (TP)	

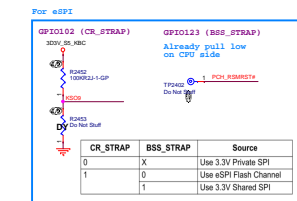
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Size	Document Number	Rev
Custom	KR CS MLK 13"	A00
Date:	Thursday, July 19, 2018	Sheet 23 of 106





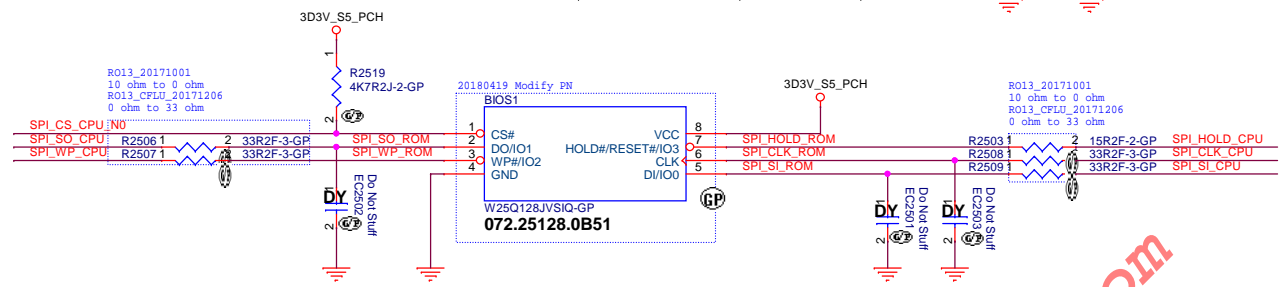
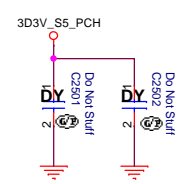
The schematic shows the power supply circuitry. It includes two diodes, R2417 and R2418, both labeled "Do Not Stuff". R2417 is connected between PROCHOST and ground. R2418 is connected between PROCHOST and the G pin of the 82N702.J31 component. The 82N702.J31 component has pins G, S, D, and EP. Pin S is connected to ground. Pin D is connected to the X pin of the PIC18F67J01, which is also connected to PROCHOST\_CPU. The PIC18F67J01 is shown with its internal components, including a diode and a capacitor. A note indicates that the PIC18F67J01 is not required for the evaluation board.



SSID = SPI Flash

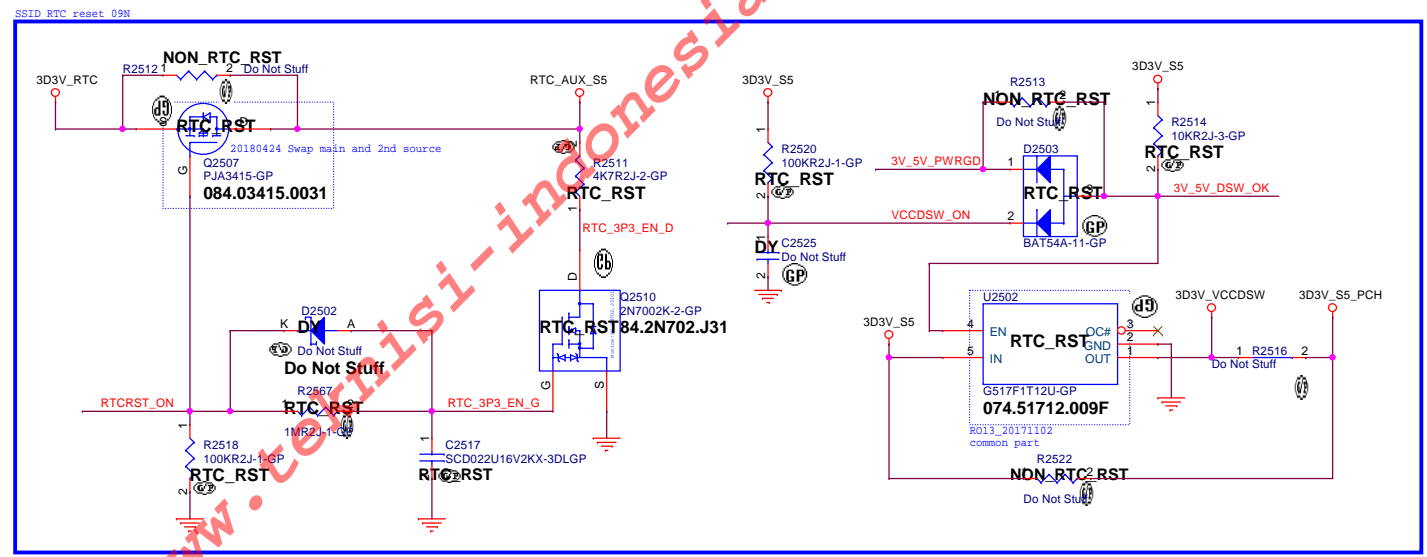
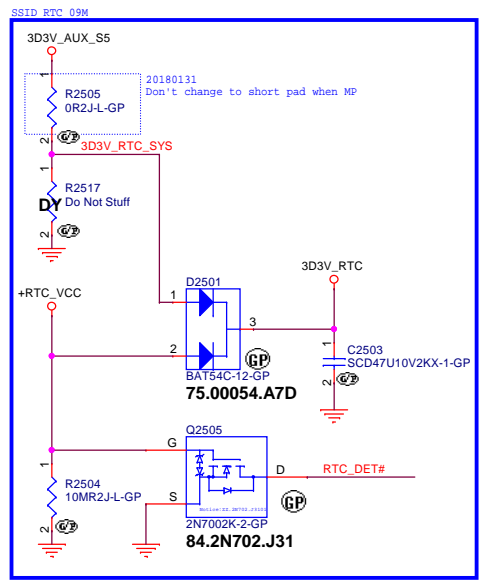
- [15,18] SPI\_HOLD\_CPU <<>>
- [18,91] SPI\_CLK\_CPU >>>
- [15,18,91] SPI\_SL\_CPU >>>
- [18] SPI\_CS\_CPU\_N0 >>>
- [18,91] SPI\_SO\_CPU <<<
- [15,18] SPI\_WP\_CPU <<>>

Source	QUAD/DUAL fast read	DUAL fast read	SFDP
72.12873.001	0	0	0
72.25128.0E1	0	0	0
	0	0	0



Main Func = RTC

- [18,24] RTCRST\_ON >>>
- [17,40,45] 3V\_5V\_PWRGD >>>
- [24] VCCDSW\_ON >>>
- [15,20] RTC\_DET# <<<
- [52,53] 3V\_5V\_DSW\_OK <<<



29.2.1 VCCRTC External Circuit

On KBL, the VCCRTC max voltage is being reduced to minimize leakage on the ESD diodes and prevent RTC oscillator problems. Whether VCCRTC is sourced from Vbat in G3 or VCCDSW\_3p3 in Non-G3 state, platform designers must ensure the effective voltage at VCCRTC does not exceed 3.2V. The following sections will detail various options platform designers can use to achieve this new specification.

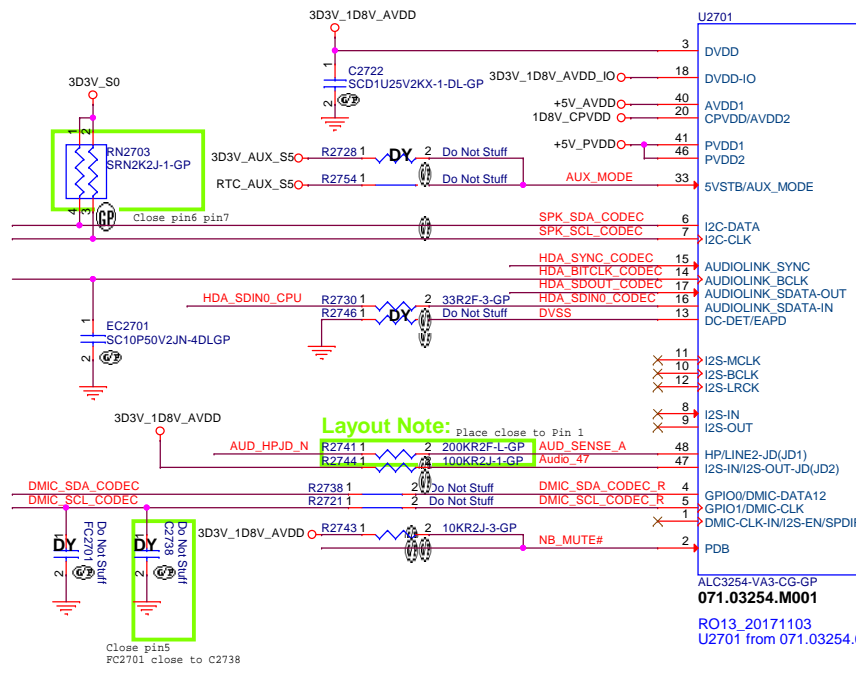




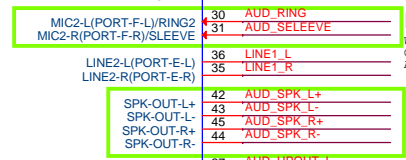


SSID = Audio

- [19] HDA\_SYNC\_CODEEC >>>
- [19] HDA\_BITCLK\_CODEEC >>>
- [19] HDA\_SDOUT\_CODEEC >>>
- [19] HDA\_SDI0\_CPU <<<
- [55] DMIC\_SCL\_CODEEC <<<
- [55] DMIC\_SDA\_CODEEC <<<
- [15,19] SPKR >>>
- [24] BEEP >>>
- [29] MIC2\_VREF0\_L <<<
- [29] MIC2\_VREF0\_R <<<
- [29] AUD\_SPK\_L+ <<<
- [29] AUD\_SPK\_L- <<<
- [29] AUD\_SPK\_R+ <<<
- [29] AUD\_SPK\_R- <<<
- [29] AUD\_RING <<<
- [29] AUD\_SELEEVE <<<
- [29] LINE1\_L <<<
- [29] LINE1\_R <<<
- [29] AUD\_HPJD\_N <<<
- [24] NB\_MUTE# <<<
- [29] AUD\_HPOUT\_L <<<
- [29] AUD\_HPOUT\_R <<<
- [29] SPK\_SCL\_CODEEC <<<
- [29] SPK\_SDA\_CODEEC <<<

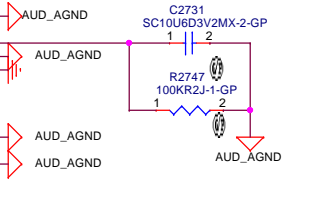


Layout Note: place close to Pin 1

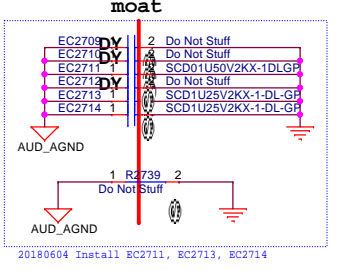
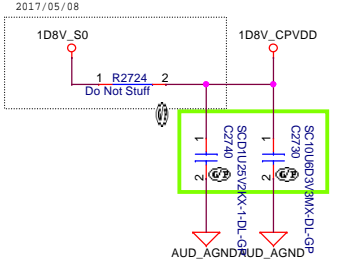
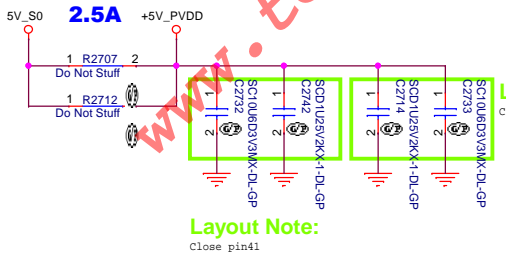
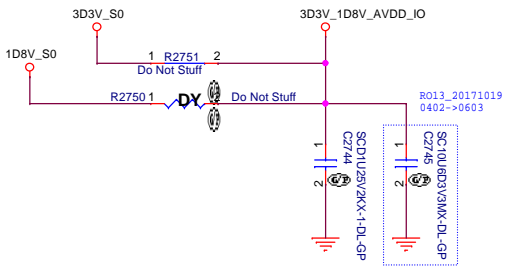
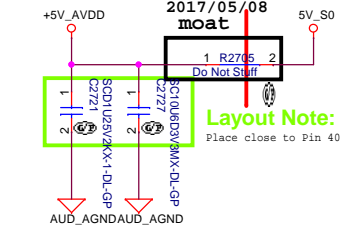
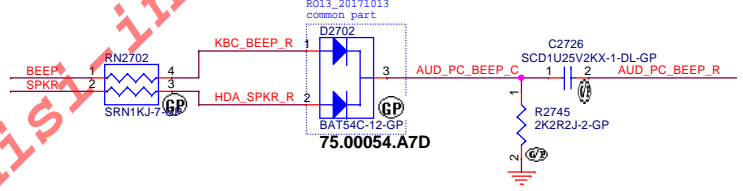
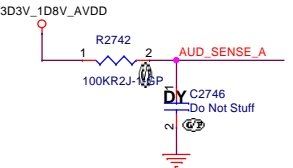
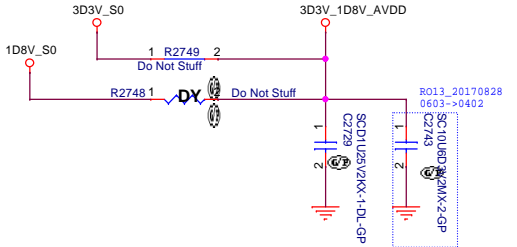


Layout Note: Width>40mil, to improve Headphone Crosstalk noise Change it to sharp will be better. Add 2 vias (>0.5A) when trace layer change.

Layout Note: Speaker trace width >40mil @ 2W4ohm speaker power



Layout Note: Place close to Pin 40



Layout Note: Close pin41

Layout Note: Close pin46

Layout Note: Close pin 20

Layout Note: R2739 should place nearby codec IC.



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Size  
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Document Number  
**KR CS MLK 13"**

Rev  
**A00**

Date: Thursday, July 19, 2018

Sheet 28 of 106



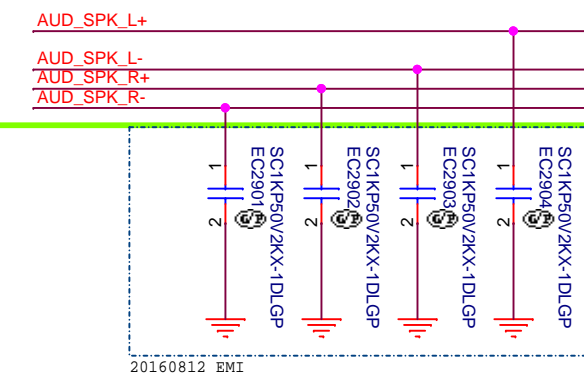
# SSID = Audio

[27] AUD\_SPK\_L+ >>>  
[27] AUD\_SPK\_L- >>>  
[27] AUD\_SPK\_R+ >>>  
[27] AUD\_SPK\_R- >>>  
[27] SPK\_SCL\_CODEC >>>  
[27] SPK\_SDA\_CODEC >>>  
[21] SPK\_ID >>>

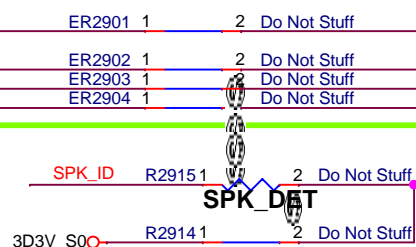
[27] MIC2\_VREFO\_R >>>  
[27] MIC2\_VREFO\_L >>>  
[27] AUD\_RING <<<  
[27] AUD\_HPOUT\_L >>>  
[27] LINE1\_L >>>  
[27] AUD\_HPOUT\_R >>>  
[27] LINE1\_R >>>  
[27] AUD\_SELEEVE <<<  
[27] AUD\_HPJD\_N <<<

## Layout Note:

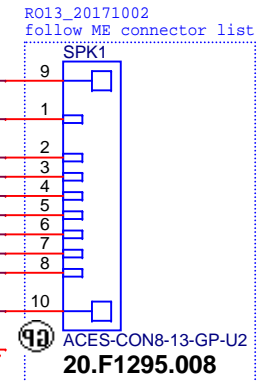
Speaker trace width >40mil @ 2W4ohm speaker power



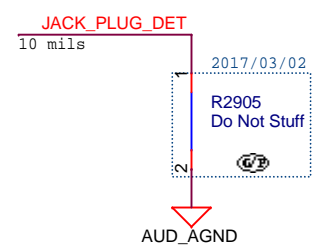
## Speaker



Function	R2914	R2915
EEPROM Speaker	0	NC
Speaker detection	10K	0

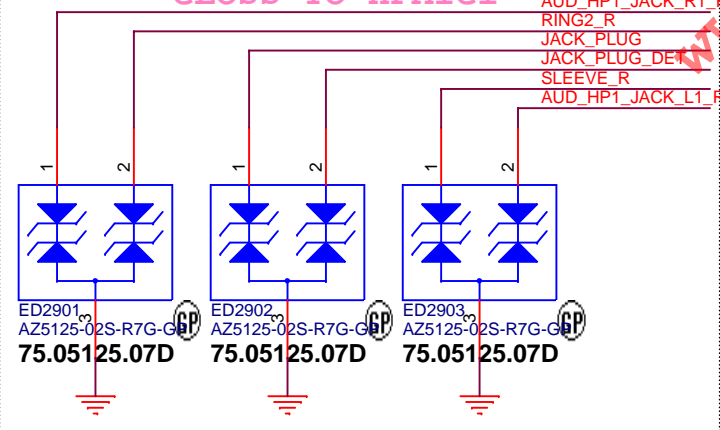


AUD\_SPK\_L- C 1 AFTP2901  
AUD\_SPK\_L+ C 1 AFTP2902  
AUD\_SPK\_R- C 1 AFTP2903  
AUD\_SPK\_R+ C 1 AFTP2904



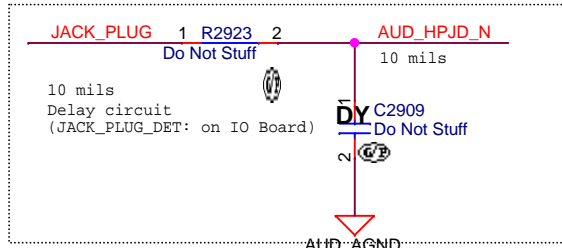
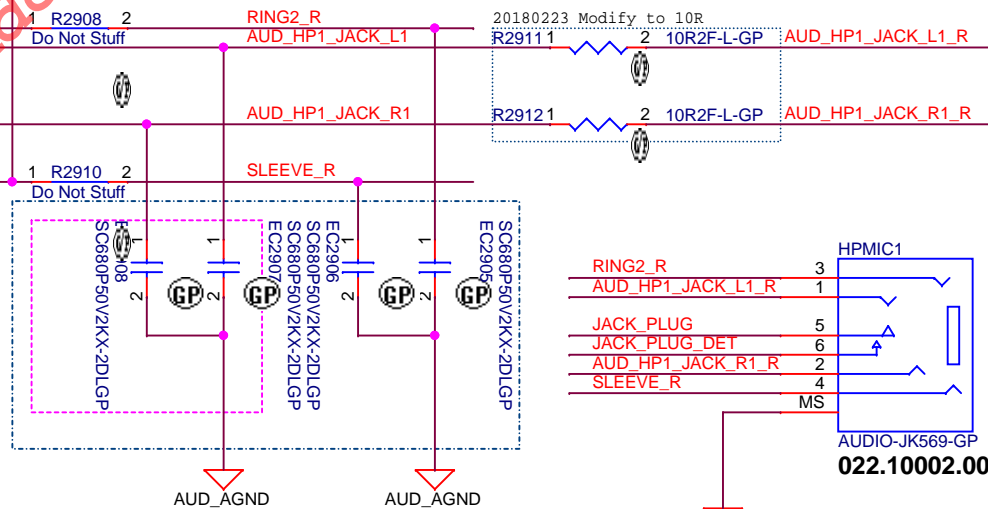
20180221 Follow KR 13 to modify ESD  
20180601 Movie TVS to close CONN.

## CLOSE TO HPMIC1



## Layout Note:

R2908 EC2907 should place nearby codec IC.



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**KR CS MLK 13"**

Rev

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Sheet 30 of 106



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**KR CS MLK 13"**

Rev  
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Sheet 31 of 106



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**KR CS MLK 13"**

Rev  
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Sheet 32 of 106



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<b>Card Reader-RTS5170</b>			
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A4	<b>KR CS MLK 13"</b>		<b>A00</b>
Date: Thursday, July 19, 2018		Sheet 33 of	106



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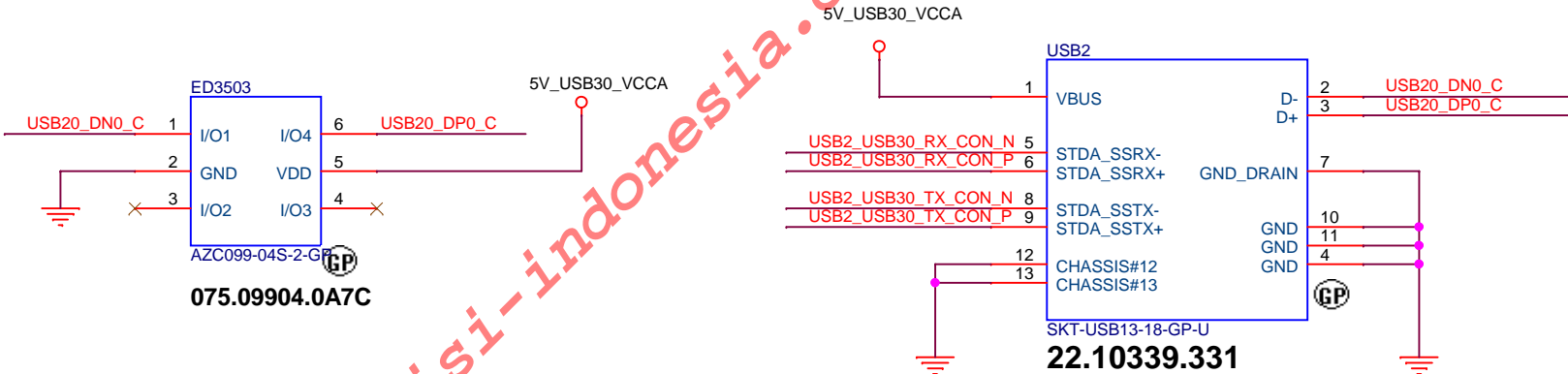
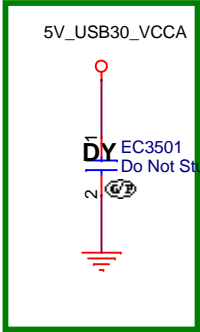
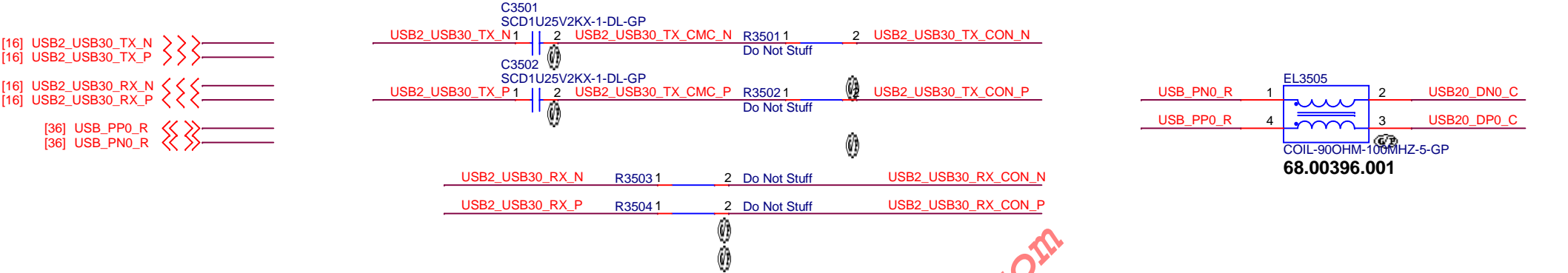
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Sheet 34 of 106

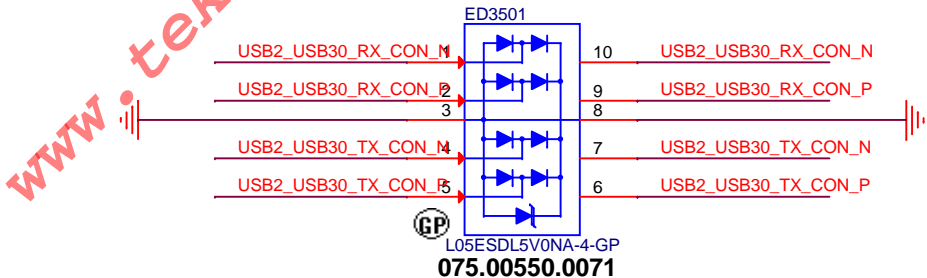


Main Func = USB3.0 Port2


USB3.0 Port2 and USB2.0 Port2



USB 3.0 Connector Pin definition	
1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX- SuperSpeed RX
6	StdA_SSRX+
7	GND
8	StdA_SSTX- SuperSpeed TX
9	StdA_SSTX+



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**USB switch**

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Sheet 35 of 106







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**KR CS MLK 13"**

Rev  
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Document Number

**KR CS MLK 13"**

Rev  
**A00**

Date: Thursday, July 19, 2018

Sheet 38 of 106



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A4

Document Number

**KR CS MLK 13"**

Rev  
**A00**

Date: Thursday, July 19, 2018

Sheet 39 of 106








SSID = Power Plane & Sequence

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Title <b>Connected_Standby(1/2)+DS3</b>					
Size A4		Document Number <b>KR CS MLK 13"</b>			Rev <b>A00</b>
Date: Thursday, July 19, 2018		Sheet 41		of 106	



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Title **Connected\_Standby(2/2)**

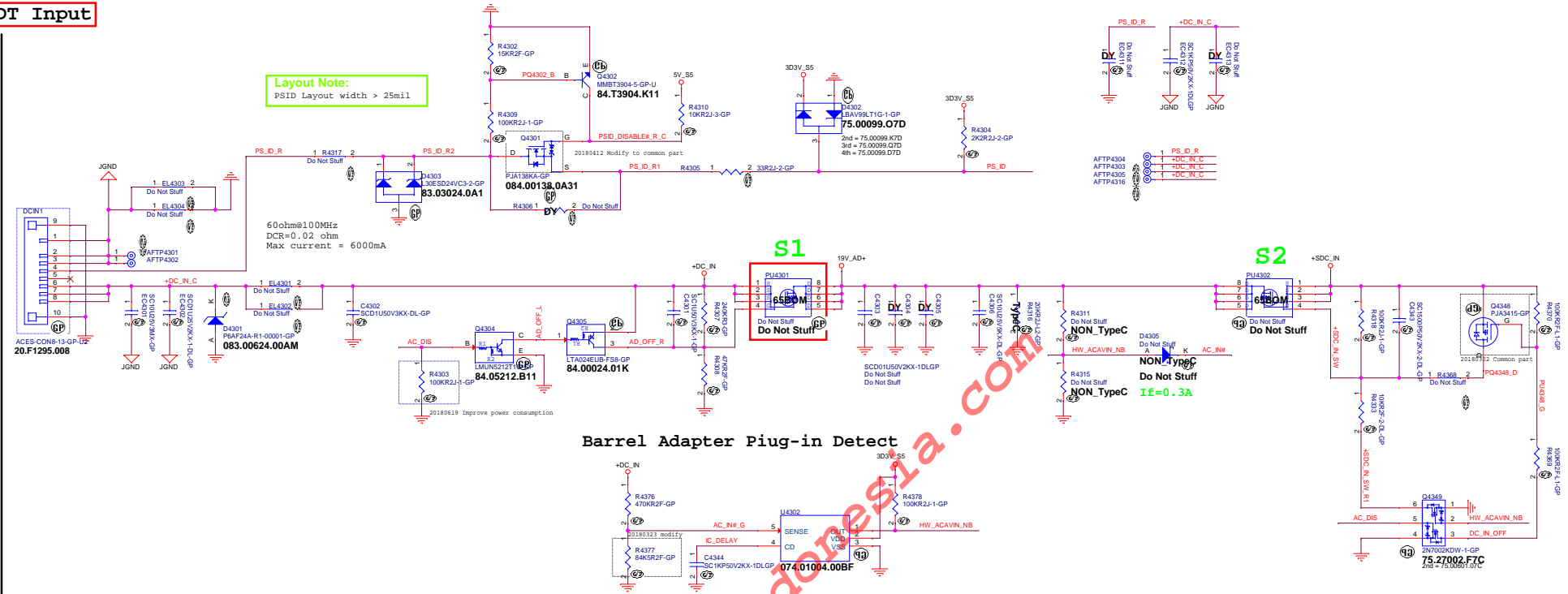
Size A4	Document Number <b>KR CS MLK 13"</b>	Rev <b>A00</b>
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Date: Thursday, July 19, 2018 Sheet 42 of 106



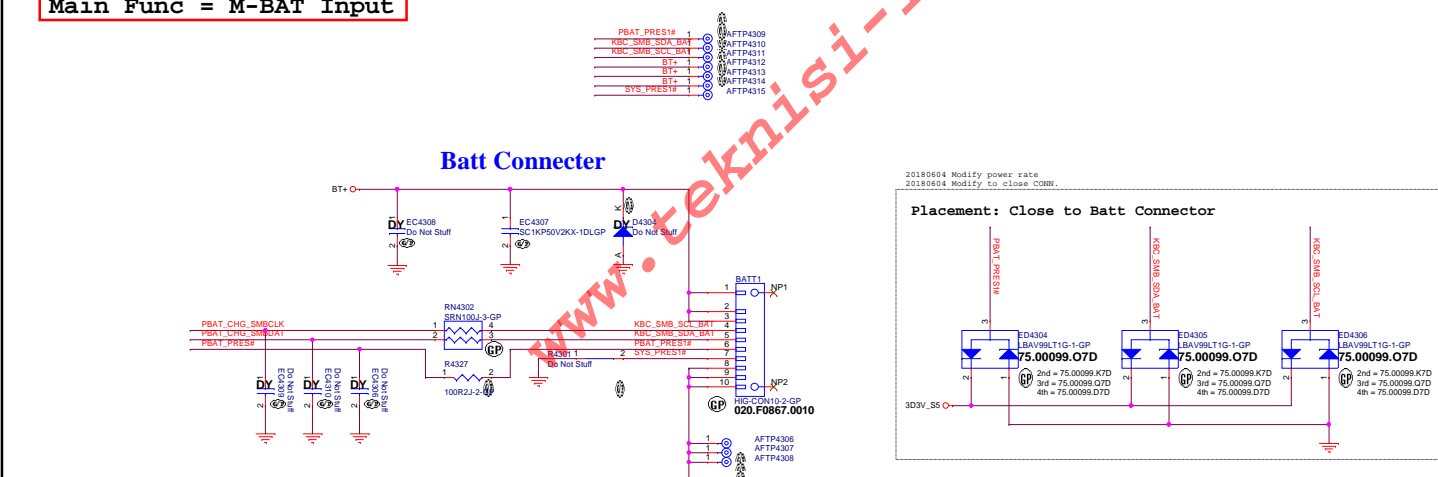
Main Func = ADT Input

[24] HW\_ACAVN\_NB <<<  
[24] PS\_ID <<<  
[17,44] AC\_INH >>>  
[24] AC\_DIS >>>



Main Func = M-BAT Input

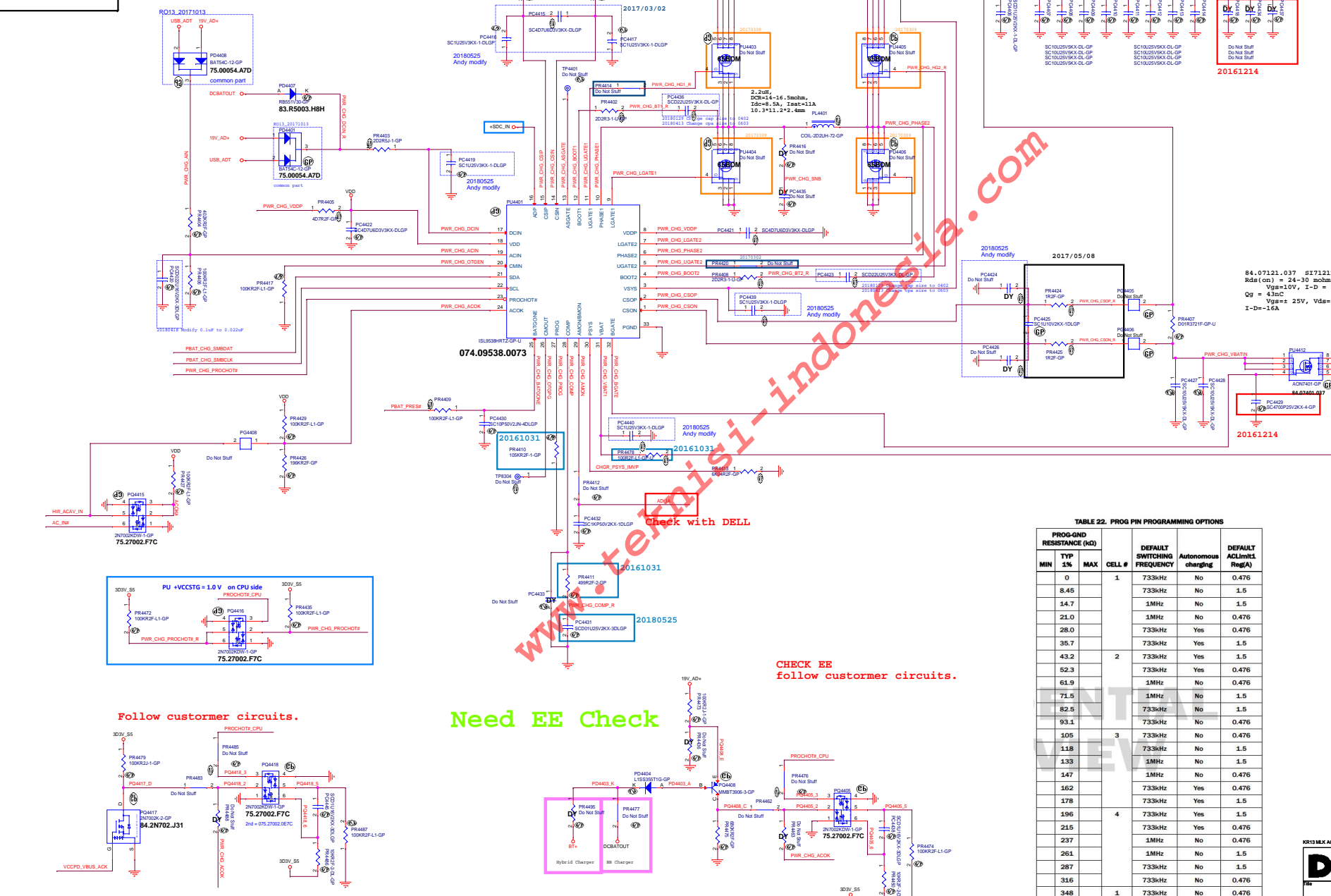
[24,44] PBAT\_CHG\_SMBCLK <<<  
[24,44] PBAT\_CHG\_SMBDAT <<<  
[24,44] PBAT\_PRESTW <<<





Main Func = Charger

[24.3] PBAT\_CHG\_SMBCLK >>>  
[24.3] PBAT\_CHG\_SMBDAT >>>  
[24.4] PROCHOTR\_CPU <<<  
[24.5] PBAT\_PRES <<<  
[24.5] HW\_ACADV\_IN <<<  
[17.4] AC\_IN <<<  
[24] AD\_IA <<<  
From NXP ACK  
[74] VCCPD\_VBUS\_ACK >>>  
[86] CHGR\_PSYS\_BVPP <<<



Follow customer circuits.

Need EE Check

CHECK EE follow customer circuits.

TABLE 22. PROG PIN PROGRAMMING OPTIONS						
PROG-GND RESISTANCE (kΩ)			CELL #	DEFAULT SWITCHING FREQUENCY	Autonomous charging	DEFAULT ACL/limit1 Reg(A)
MIN	TYP 1%	MAX				
	0		1	733kHz	No	0.476
	8.45			733kHz	No	1.5
	14.7			1MHz	No	1.5
	21.0			1MHz	No	0.476
	28.0			733kHz	Yes	0.476
	35.7			733kHz	Yes	1.5
	43.2		2	733kHz	Yes	1.5
	52.3			733kHz	Yes	0.476
	61.9			1MHz	No	0.476
	71.5			1MHz	No	1.5
	82.5			733kHz	No	1.5
	93.1			733kHz	No	0.476
	105		3	733kHz	No	0.476
	118			733kHz	No	1.5
	133			1MHz	No	1.5
	147			1MHz	No	0.476
	162			733kHz	Yes	0.476
	178			733kHz	Yes	1.5
	196		4	733kHz	Yes	1.5
	215			733kHz	Yes	0.476
	237			1MHz	No	0.476
	261			1MHz	No	1.5
	287			733kHz	No	1.5
	316			733kHz	No	0.476
	348		1	733kHz	No	0.476

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Charger

Document Number

KR CS MLK 13"

Date: Thursday, 20/11/2018

Page: 46 of 46

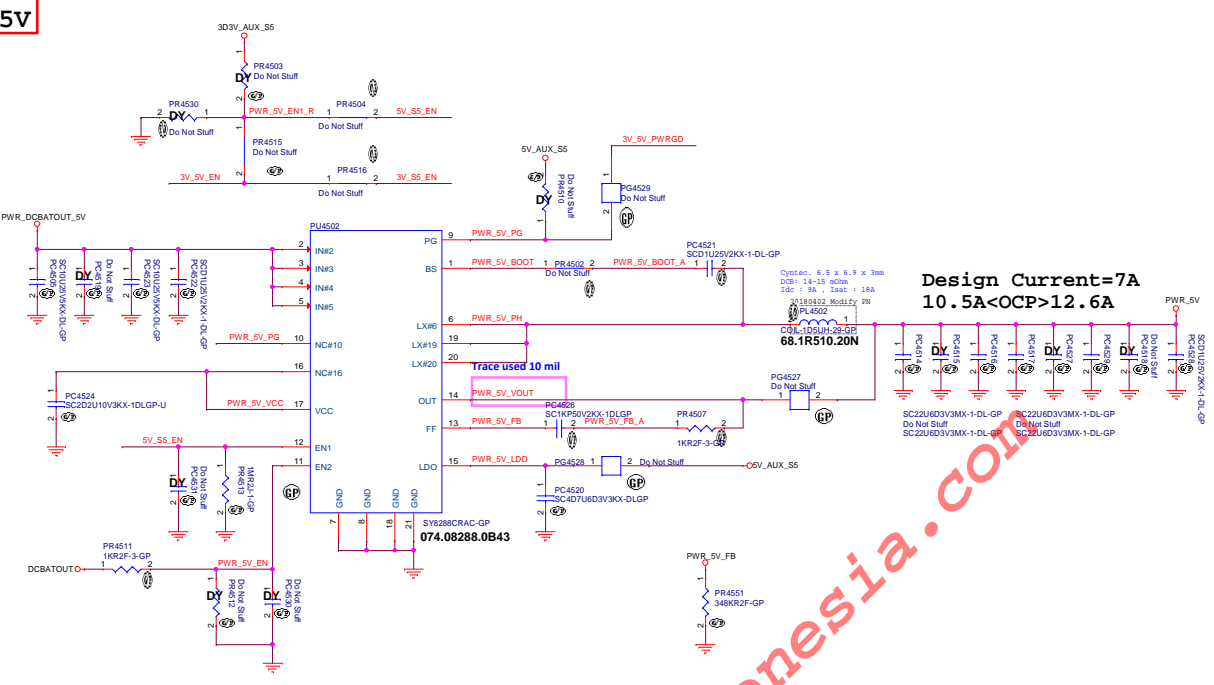


SSID = PWR.Plane.Regulator\_5V

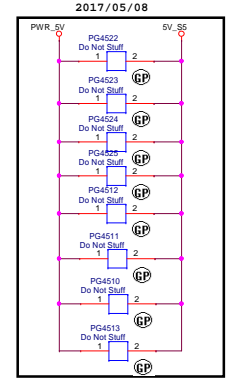
[40] 3V\_SV\_EN >>>  
[17,25,40] 3V\_SV\_PWRGD <<<



EN rating 25V  
EN Rising Threshold : 0.8V  
Ilimt : 8A



Design Current=7A  
10.5A<OCP>12.6A

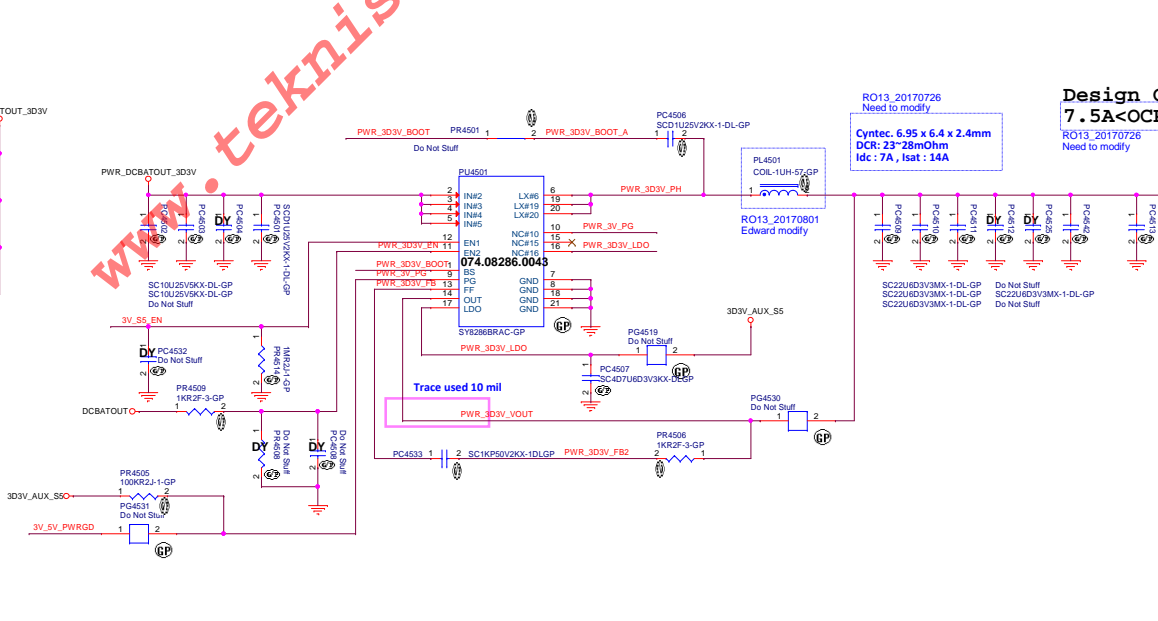


2017/05/08

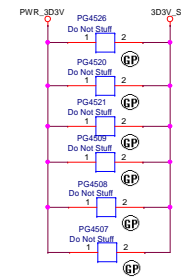
SSID = PWR.Plane.Regulator\_3D3V



EN rating 25V  
EN Rising Threshold : 0.8V  
Ilimt : 8A

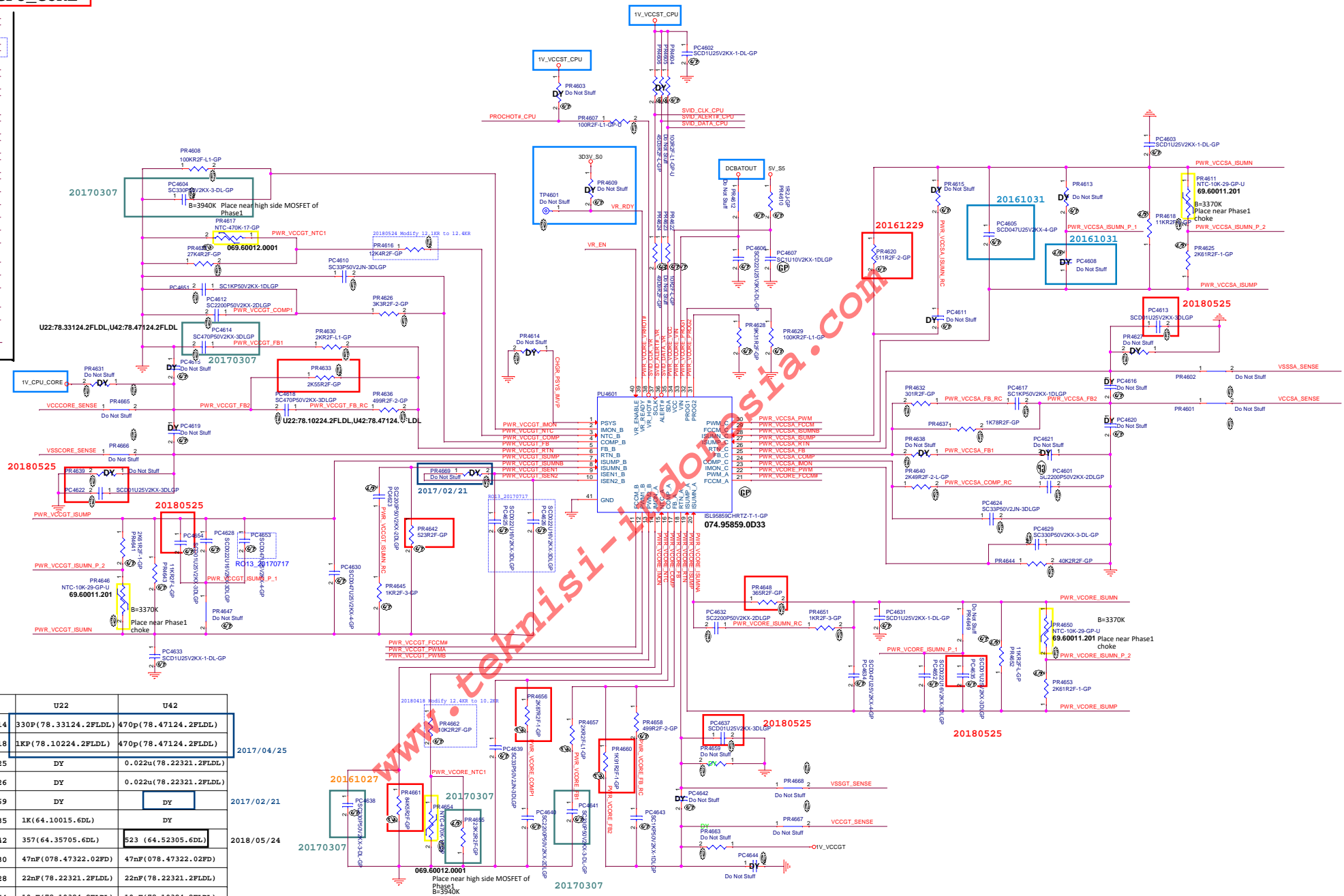


Design Current=8A  
7.5A<OCP>9A





[7]	VCCORE_SENSE	<<<
[7]	VSSCORE_SENSE	<<<
[48]	PWR_VCGGT_ISEN1	>>>
[48]	PWR_VCGGT_ISEN0	>>>
[48]	PWR_VCGGT_ISUMP	>>>
[48]	PWR_VCGGT_ISUMN	>>>
[47]	PWR_VCORE_ISUMP	>>>
[47]	PWR_VCORE_ISUMN	>>>
[8]	VCGGT_SENSE	<<<
[8]	VSSGT_SENSE	<<<
[8]	VCCSA_SENSE	<<<
[8]	VSSSA_SENSE	<<<
[50]	PWR_VCCSA_ISUMP	>>>
[50]	PWR_VCCSA_ISUMN	>>>
[48]	PWR_VCGGT_PWMA	>>>
[48]	PWR_VCGGT_PWMB	>>>
[48]	PWR_VCGGT_FCCMA	>>>
[47]	PWR_VCORE_FCCMA	>>>
[50]	PWR_VCCSA_FCCM	>>>
[50]	PWR_VCCSA_PWM	>>>
[47]	PWR_VCORE_PWM	>>>
[7]	SVID_CLK_CPU	<<<
[7]	SVID_ALERT#_CLK	<<<
[7]	SVID_DATA_CPU	<<<
[2,44]	PROCHOT#_CPU	<<<
[40]	VR_EN	>>>
[44]	CHGR_PSYS_MV	>>>

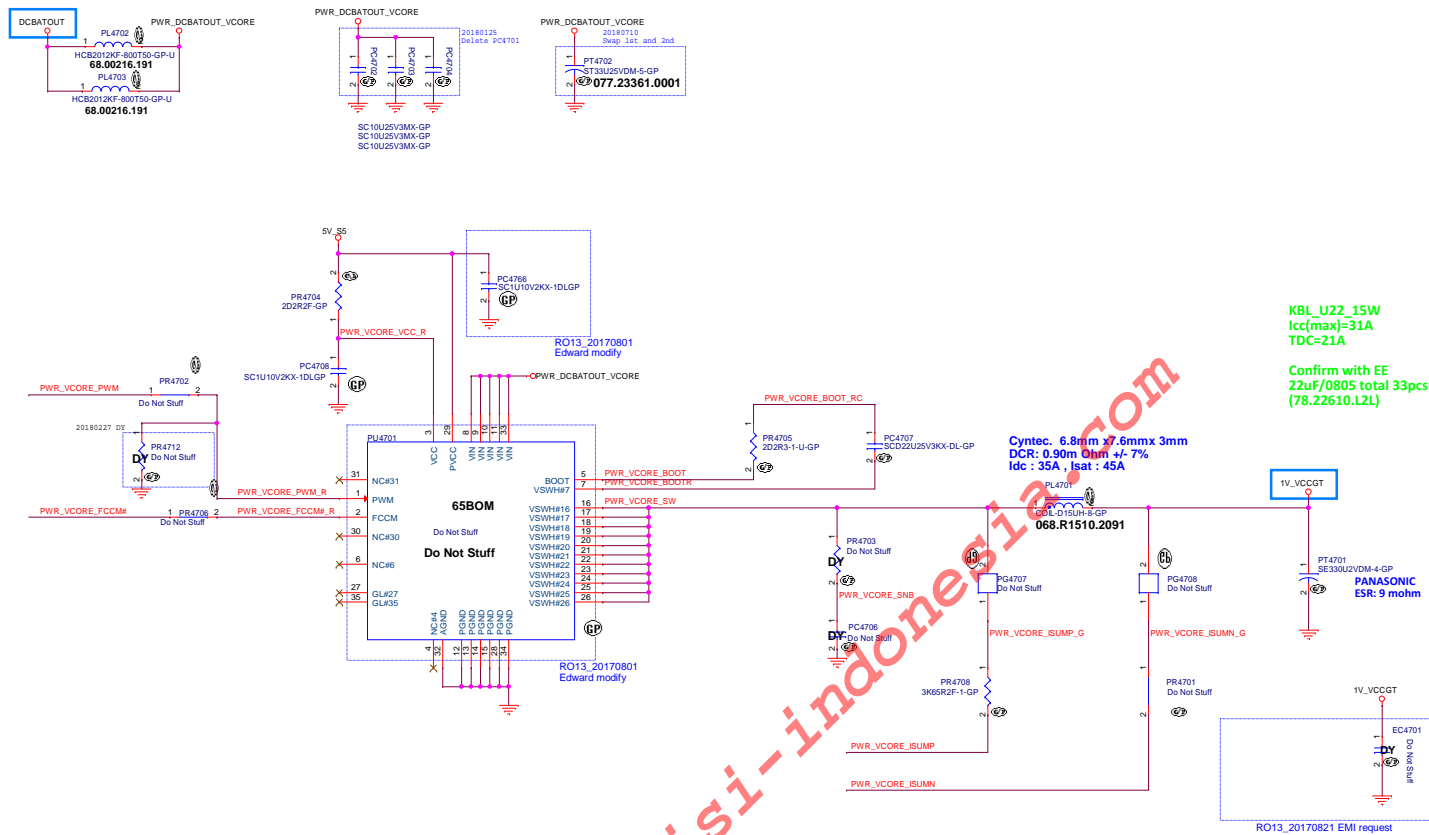


	U22	U42	
PC4614	330P(78.33124.2FLDL)	470p(78.47124.2FLDL)	2017/04/21
PC4618	1KP(78.10224.2FLDL)	470p(78.47124.2FLDL)	
PC4625	DY	0.022u(78.22321.2FLDL)	
PC4626	DY	0.022u(78.22321.2FLDL)	2017/02/21
PR4669	DY	DY	
PR4635	1K(64.10015.6DL)	DY	
PR4642	357(64.35705.6DL)	523 (64.52305.6DL)	2018/05/24
PC4630	47nF(078.47322.02FD)	47nF(078.47322.02FD)	2018/05/24
PC4628	22nF(78.22321.2FLDL)	22nF(78.22321.2FLDL)	
PC4654	10nF(78.10324.2FLDL)	10nF(78.10324.2FLDL)	
PC4653	DY	47nF(078.47322.02FD)	2018/05/24
PR4633	1.54K(64.15415.6DL)	2.55K(64.25515.6DL)	
PR4608	90.9K(64.90925.6DL)	100K (64.10035.6DL)	



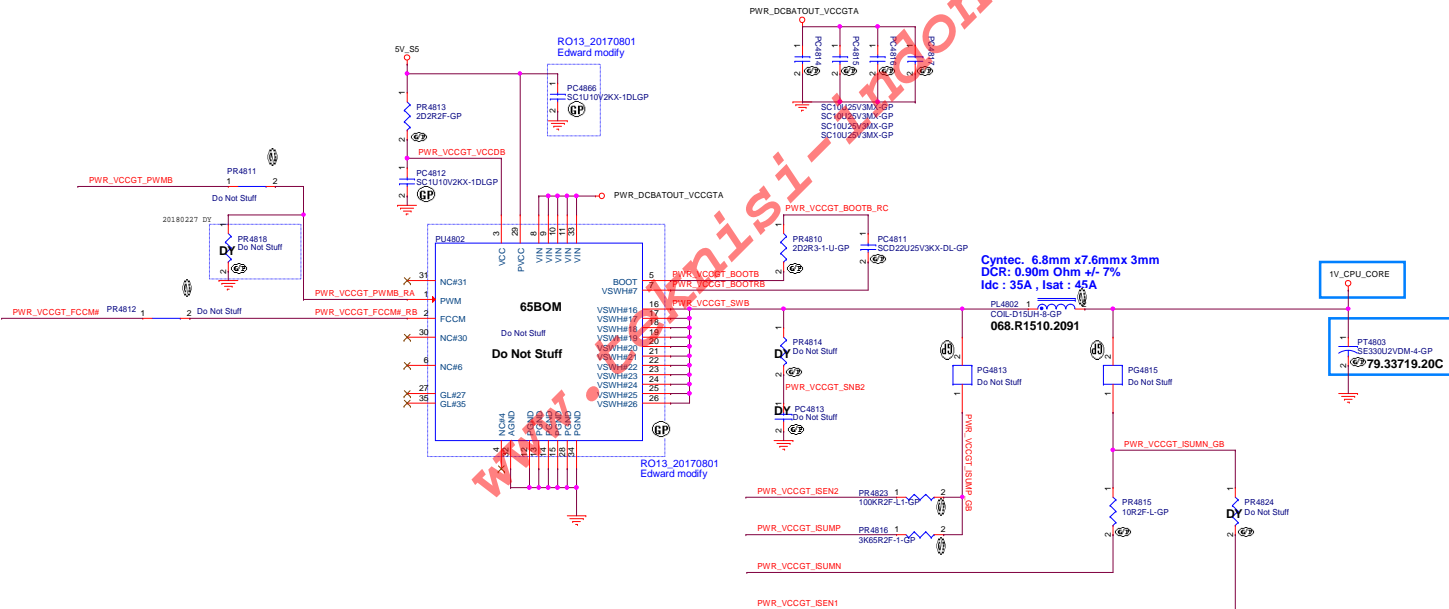
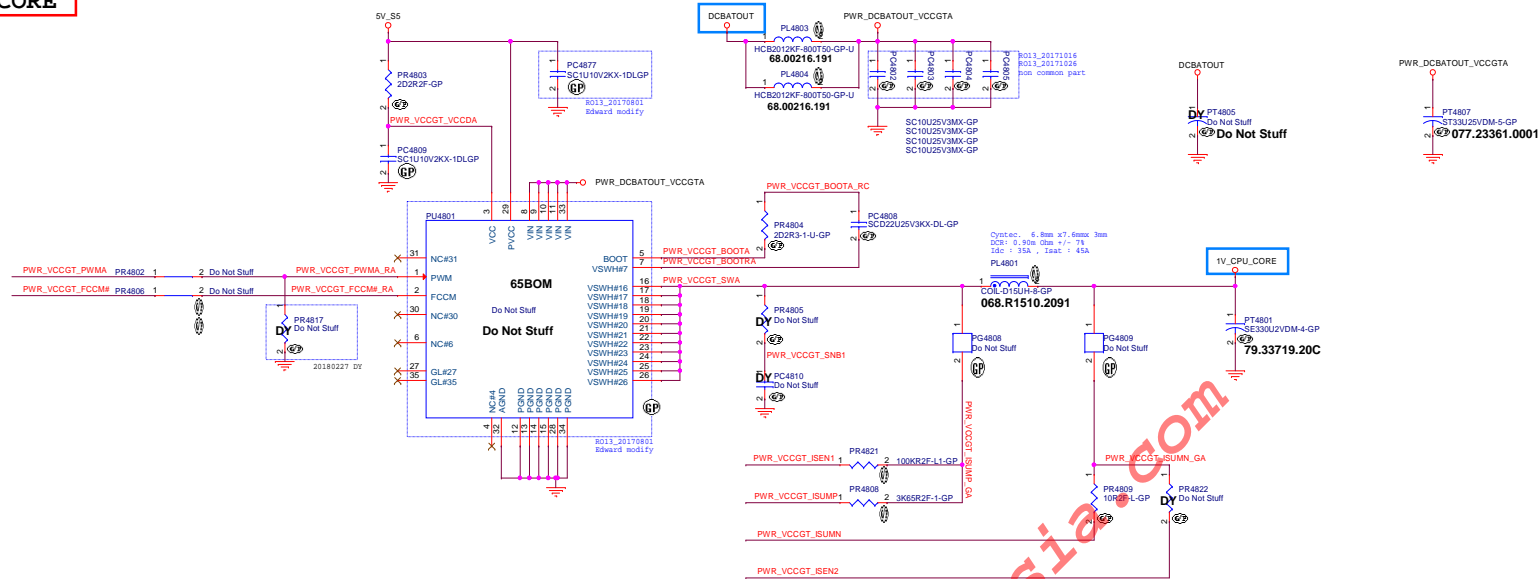
```
[46] PWR_VCORE_PWM      >>> _____
[46] PWR_VCORE_FCCM#     >>> _____

[46] PWR_VCORE_ISUMP     <<< _____
[46] PWR_VCORE_ISUMN     <<< _____
```





Main Func = CPU\_CORE



KBL-R\_U42\_15W  
Icc(max)=64A  
TDC=42A

Confirm with EE  
22uF/0805 total 36pcs  
(78.22610.L2L)

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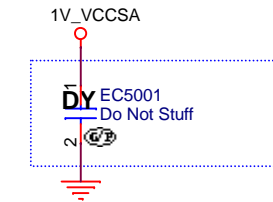
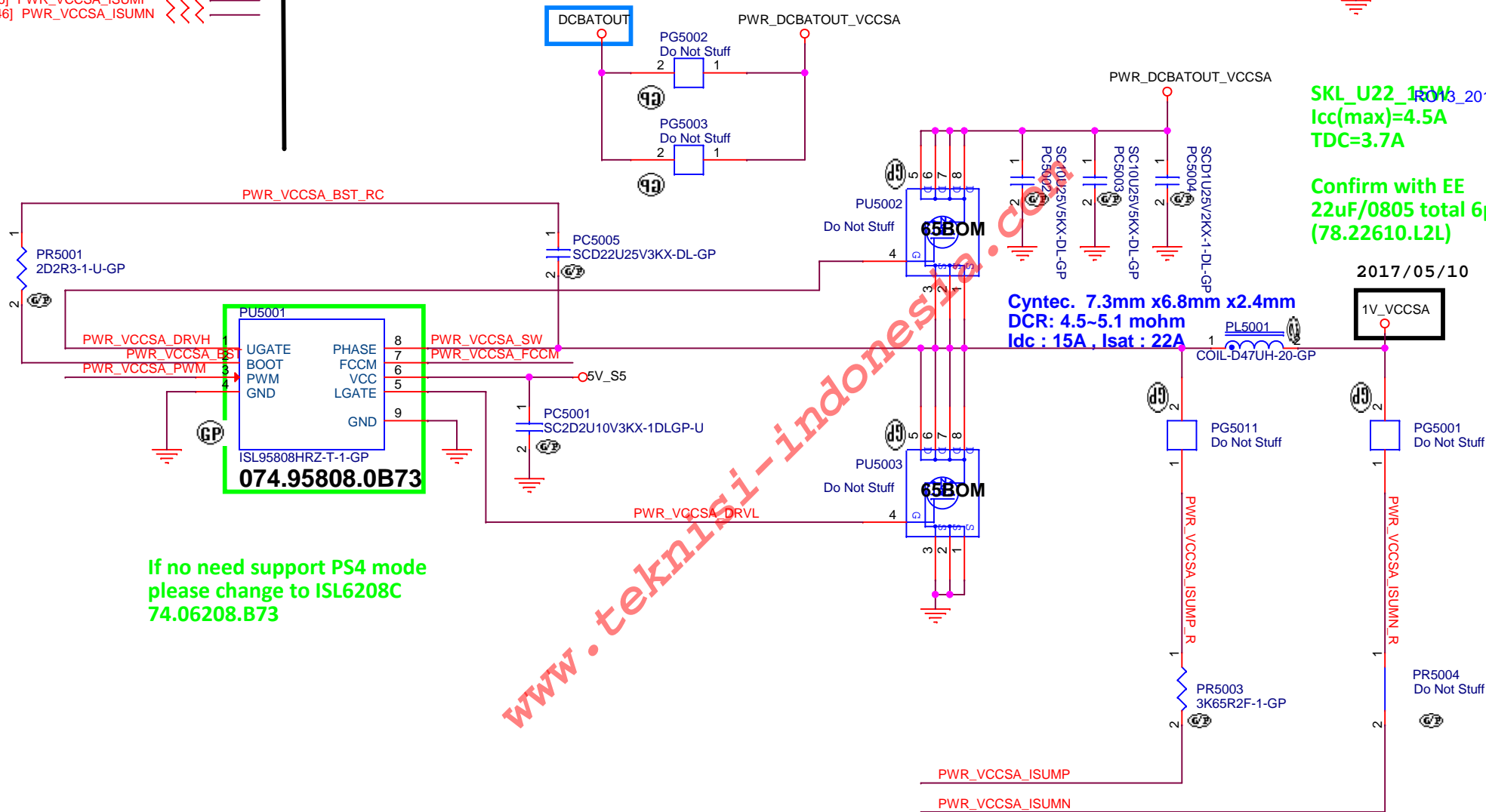
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Title <b>NCP81210MN_CPU_VCCGTUS</b>		
Size A4	Document Number <b>KR CS MLK 13"</b>	Rev <b>A00</b>
Date: Thursday, July 19, 2018		Sheet 49 of 106



SSID = CPU\_CORE

[46] PWR\_VCCSA\_PWM  
[46] PWR\_VCCSA\_FCCM  
[46] PWR\_VCCSA\_ISUMP  
[46] PWR\_VCCSA\_ISUMN



SKL\_U22\_15W Rom3\_20170821 EMI request

Icc(max)=4.5A  
TDC=3.7A

Confirm with EE  
22uF/0805 total 6pcs  
(78.22610.L2L)

2017/05/10



If no need support PS4 mode  
please change to ISL6208C  
74.06208.B73

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Title

**VCCSA**

Size  
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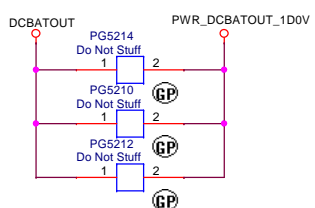
Sheet 50 of 106



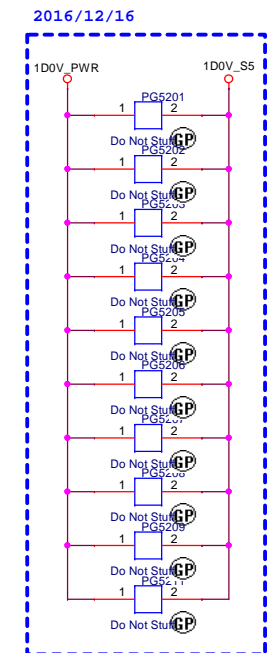
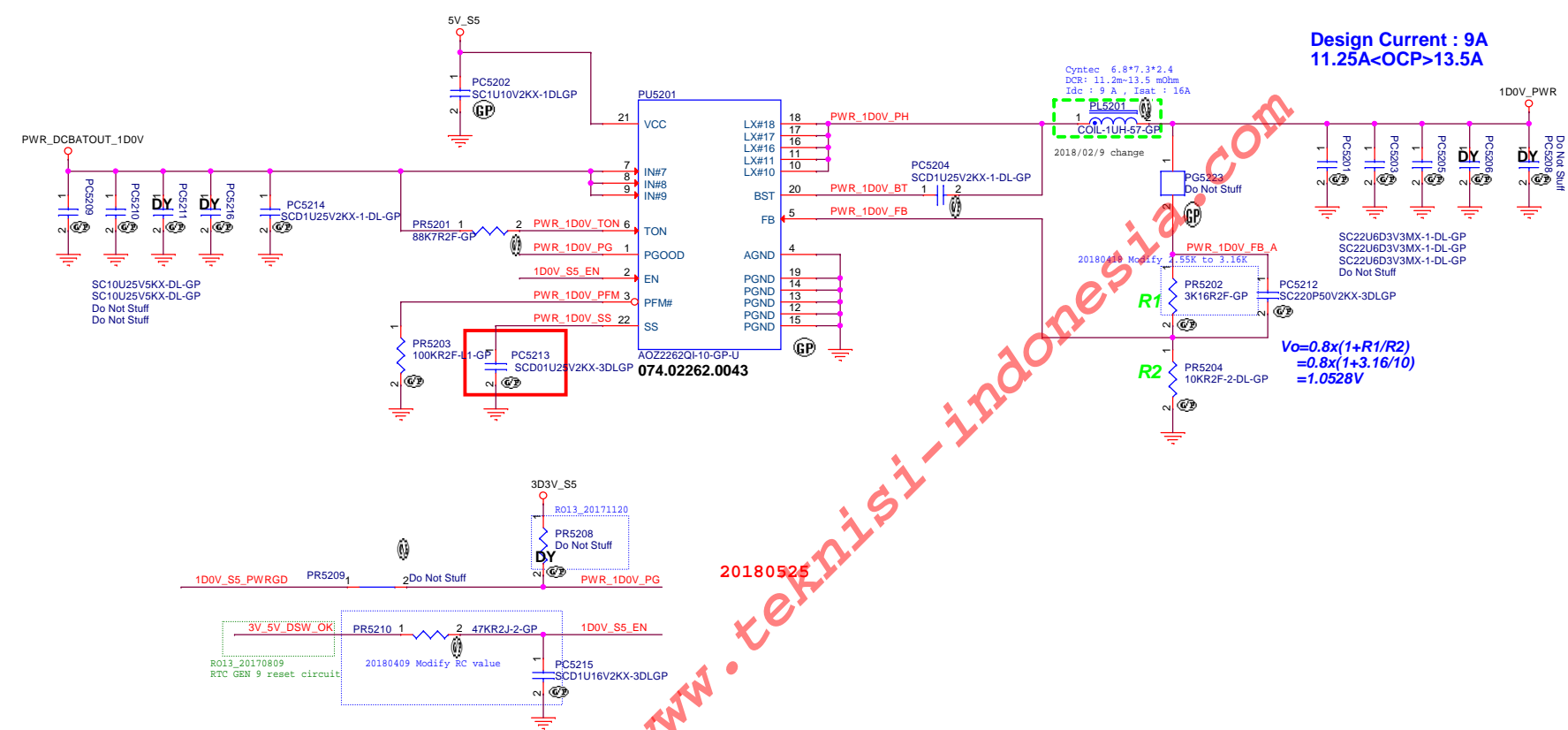




[40] 1D0V\_S5\_PWRGD <<<  
[25,53] 3V\_5V\_DSW\_OK >>>



# AOZ2262 for 1D0V

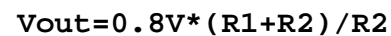
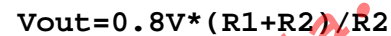


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[51] 2D5V\_S3\_PWRGD <<< \_\_\_\_\_  
 [17,40] PM\_SLP\_S4# >>> \_\_\_\_\_

[24,40] PRIM\_PWRGD <<< \_\_\_\_\_  
 [25,52] 3V\_5V\_DSW\_OK >>> \_\_\_\_\_



Sheet 53 of 106



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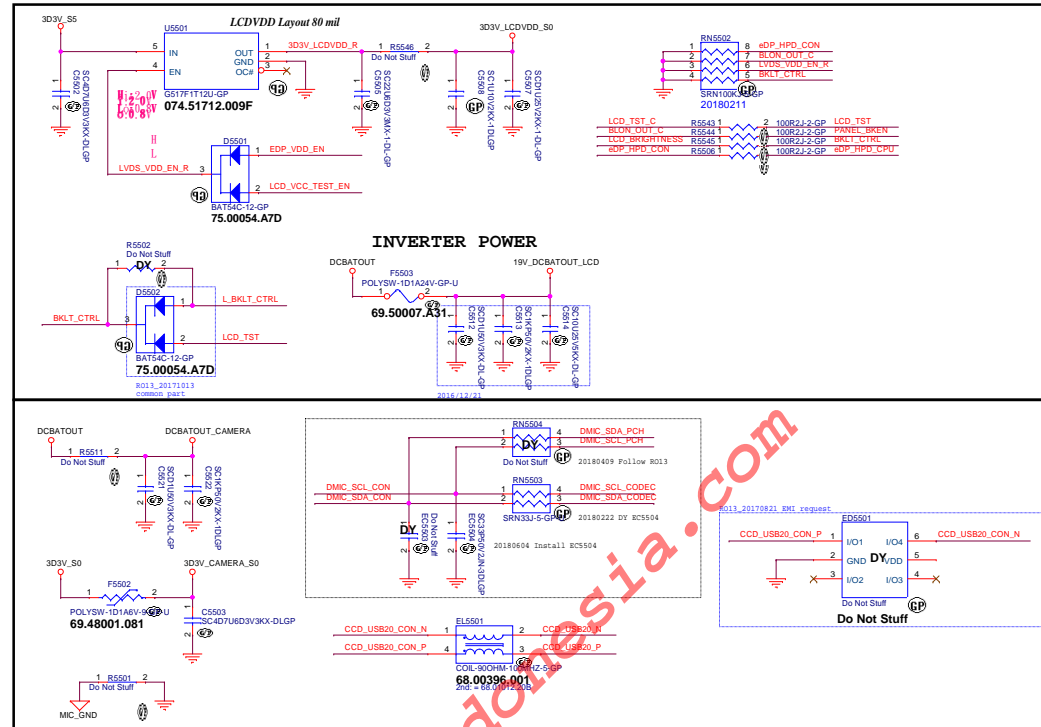
**A00**

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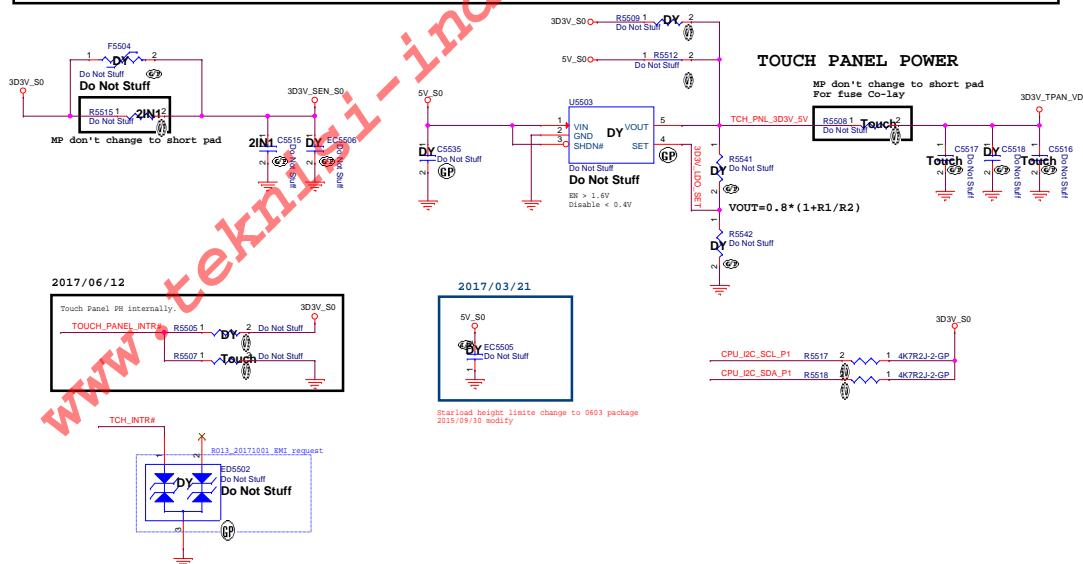
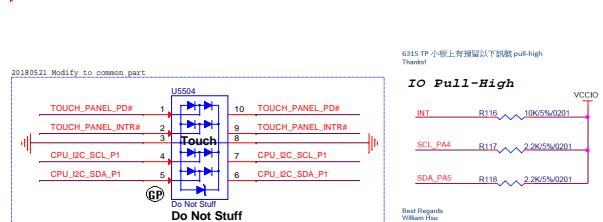
Sheet 54 of 106



**eDP Panel / HD Camera**



Pin 1-22 connection diagram for the TCR01 module. The diagram shows connections for pins 1 through 22. Pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, and 22 are shown. Connections include: Pin 1 to 3D3V\_SEN\_S0; Pin 2 to CPU\_ICC\_SDA\_ISH; Pin 3 to CPU\_ICC\_SCL\_ISH; Pin 4 to GSEN\_INT1; Pin 5 to GSEN\_INT2; Pin 6 to GYRO\_INT; Pin 7 to R5524 1; Pin 8 to GYRO\_READY; Pin 9 to R5524 2; Pin 10 to GYRO\_INT\_C; Pin 11 to TOUCH\_DETECT; Pin 12 to TOUCH\_REPORT\_SW; Pin 13 to TOUCH\_PANEL\_VCF; Pin 14 to TOUCH\_PANEL\_INT#; Pin 15 to CPU\_ICC\_SDA\_TS; Pin 16 to CPU\_ICC\_SCL\_TS; Pin 17 to CPU\_ICC\_SDA\_TS; Pin 18 to CPU\_ICC\_SCL\_TS; Pin 19 to CPU\_ICC\_SDA\_TS; Pin 20 to CPU\_ICC\_SCL\_TS; Pin 21 to 3D3V\_TSPAN\_VDD; Pin 22 to Do Not Stuff. The diagram also shows connections to TCR01, Touch, and Do Not Stuff.





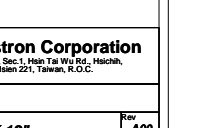
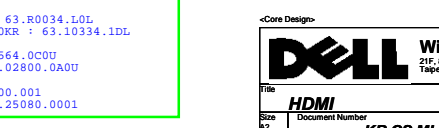
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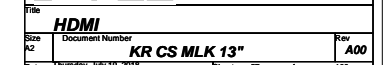
		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>CRT</b>			
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## Manual BOM control

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Date: Thursday, July 19, 2018		Sheet 58 of	106



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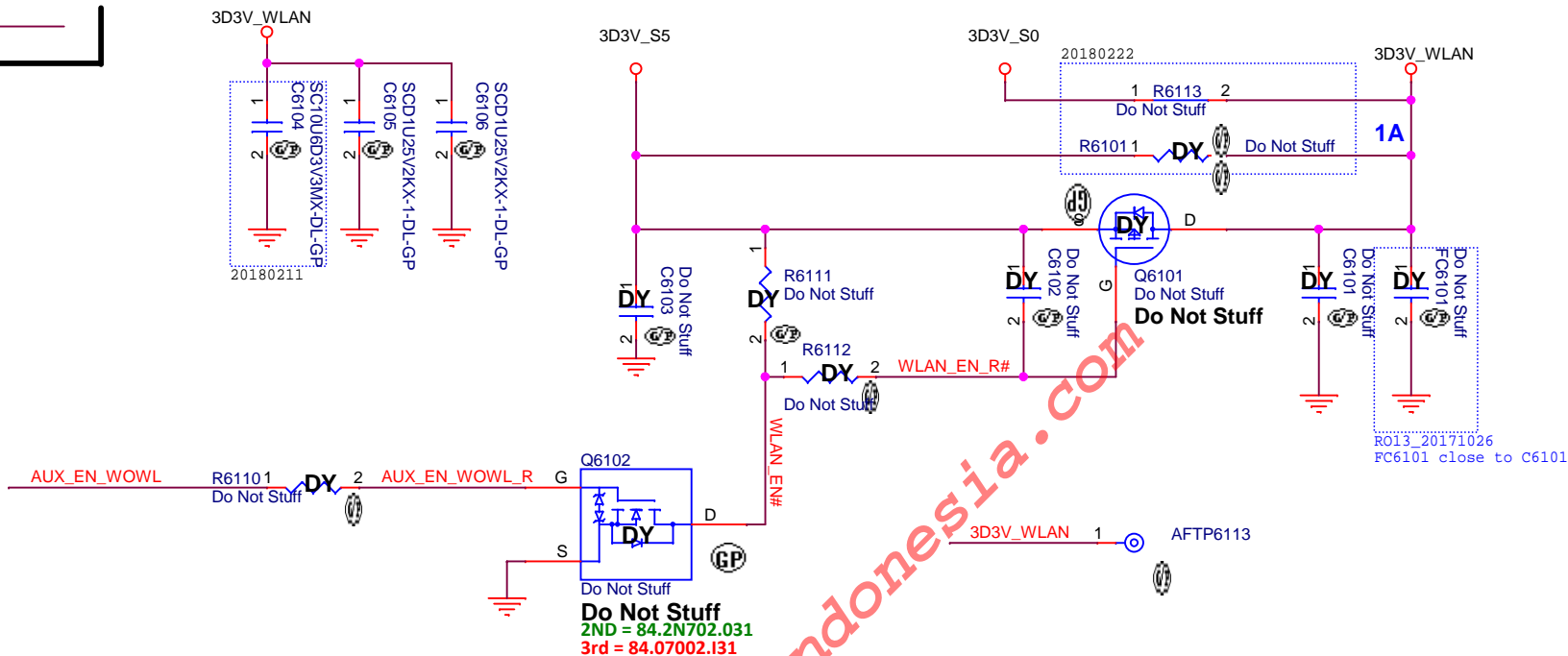
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Sheet 60 of 106



SSID = WLAN

[17,24] AUX\_EN\_WOWL>>>



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Title

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A4

Document Number

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Sheet 61 of 106



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Date: Thursday, July 19, 2018		Sheet 62 of	106



SSID = M.2

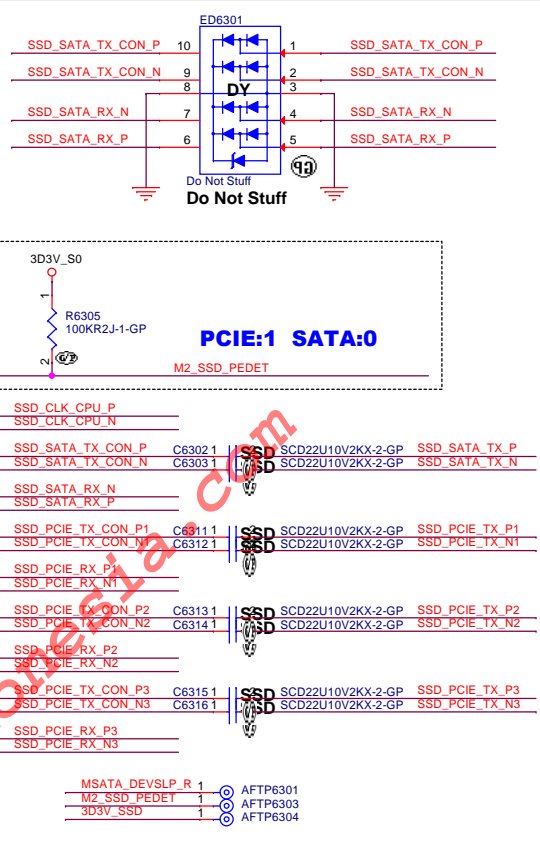
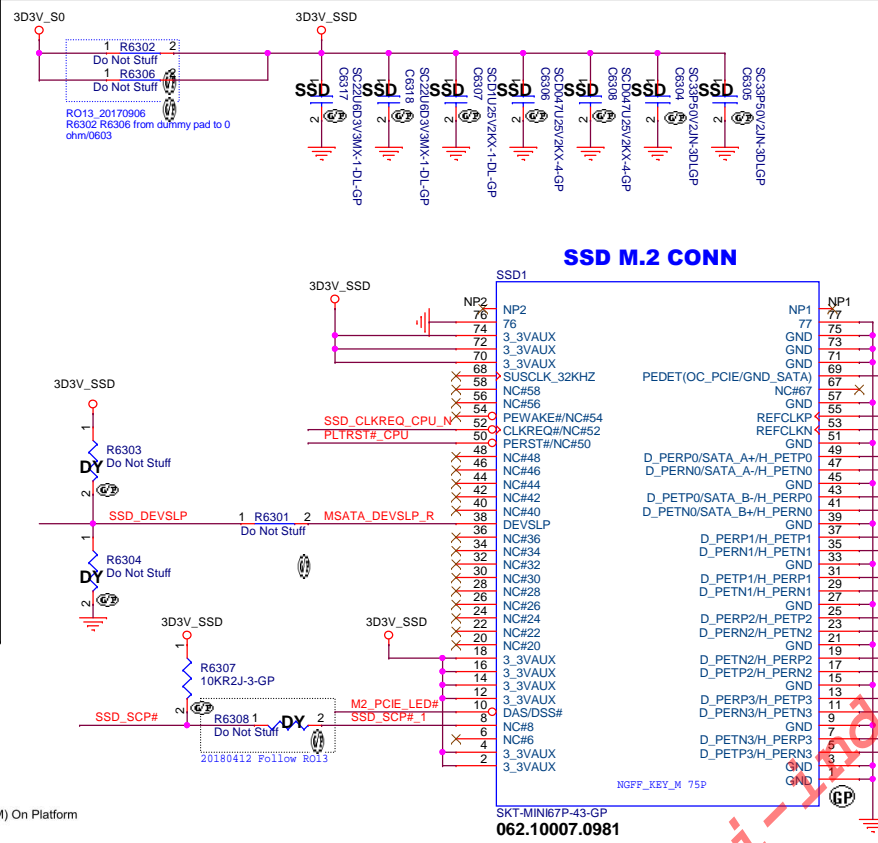
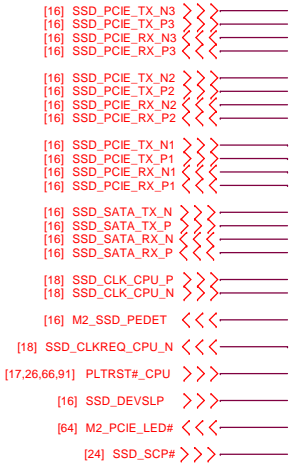


Table 48. Socket 3 SSD Pin-Out (Mechanical Key M) On Platform

74	SSD_PCIE_TX_N3	SSD_PCIE_TX_P3	SSD_PCIE_RX_N3	SSD_PCIE_RX_P3	SSD_PCIE_TX_N2	SSD_PCIE_TX_P2	SSD_PCIE_RX_N2	SSD_PCIE_RX_P2	SSD_PCIE_TX_N1	SSD_PCIE_TX_P1	SSD_PCIE_RX_N1	SSD_PCIE_RX_P1	SSD_SATA_TX_N	SSD_SATA_TX_P	SSD_SATA_RX_N	SSD_SATA_RX_P	SSD_CLK_CPU_P	SSD_CLK_CPU_N	M2_SSD_PEDET	SSD_CLKREQ_CPU_N	SSD_DEVSLP	M2_PCIE_LED#	SSD_SCP#
75	SSD_PCIE_TX_N3	SSD_PCIE_TX_P3	SSD_PCIE_RX_N3	SSD_PCIE_RX_P3	SSD_PCIE_TX_N2	SSD_PCIE_TX_P2	SSD_PCIE_RX_N2	SSD_PCIE_RX_P2	SSD_PCIE_TX_N1	SSD_PCIE_TX_P1	SSD_PCIE_RX_N1	SSD_PCIE_RX_P1	SSD_SATA_TX_N	SSD_SATA_TX_P	SSD_SATA_RX_N	SSD_SATA_RX_P	SSD_CLK_CPU_P	SSD_CLK_CPU_N	M2_SSD_PEDET	SSD_CLKREQ_CPU_N	SSD_DEVSLP	M2_PCIE_LED#	SSD_SCP#
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Table 13-11.SATA / PCI Express\* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2 / SATA	PCI Express* Gen 3 / SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF <sup>2</sup>	None	None <sup>3</sup>

**Notes:**

- Design Constraint: For PCIe only application, refer to the PCIe guidelines for details.
- Design Constraint: For SATA only application, both Tx and Rx channels need to have 10 nF capacitors on the motherboard. This option supports all SATA devices. However, the Rx 10 nF capacitor can be removed if DC coupled ODDs / devices are NOT used.
- Design Constraint: For PCIe\* Gen 2/ SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
- Design Constraint: For PCIe\* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
- Design Constraints, Required: Refer to the Chapter 3, "General Differential Signals Design Guidelines" along with the additional guidelines in this section for all design optimization guidelines.
- Design Constraint: For PCIe\* lane that needs to support either PCIe\* Gen2 devices or PCIe\* Gen3 devices, follow the PCIe\* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**

**Important!** SATA Host DEVSLP signals shall not be terminated since device shall terminate the signal.

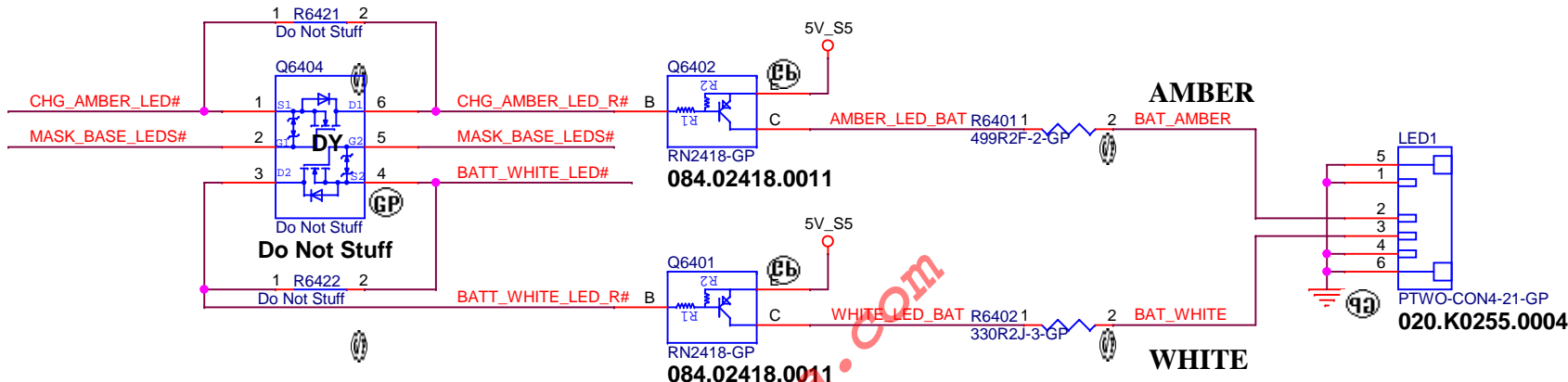
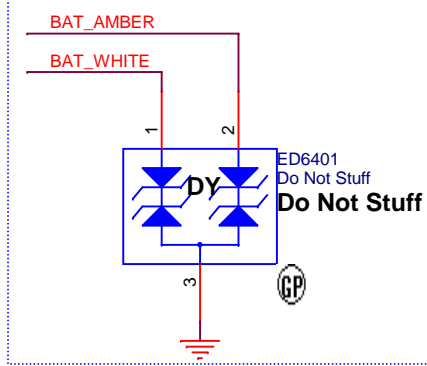
- This is an open-drain pin on the PCH side. PCH will tri-state this pin to signal to the SATA device that it may enter a lower power state (pin will go high due to pull-up that's internal to the SATA device, per DEVSLP specification). PCH will drive pin low to signal an exit from DEVSLP state.
- When used as DEVSLP, no external pull-up or pull-down termination required from SATA Host DEVSLP.



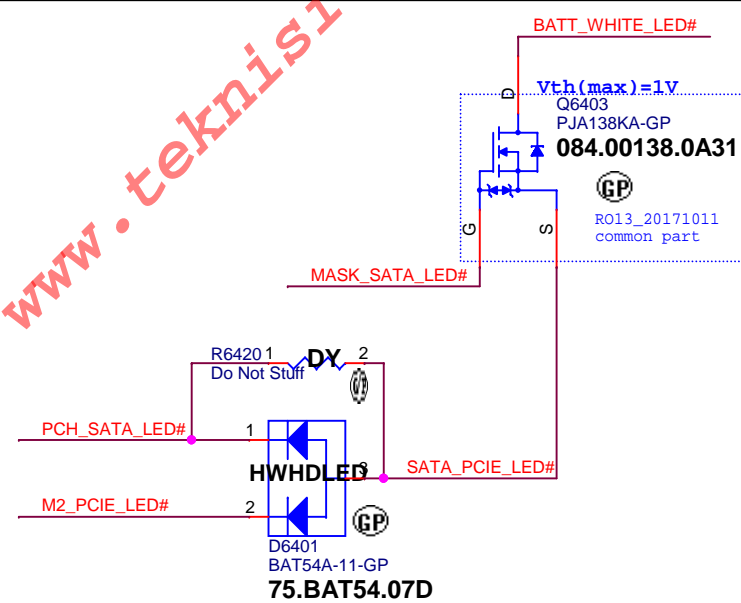
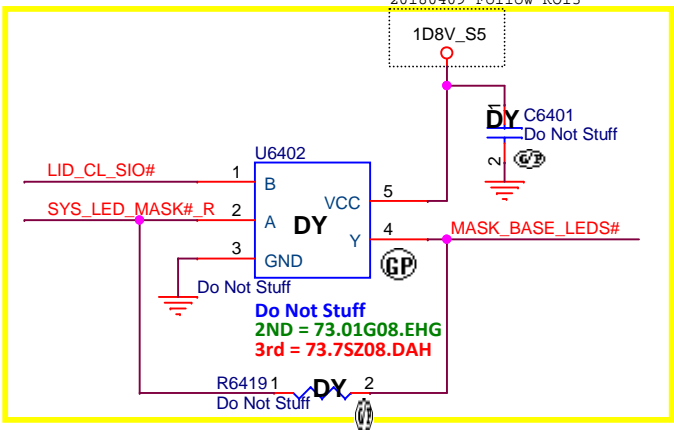
# SSID = Power BTN

[24] CHG\_AMBER\_LED# >>> \_\_\_\_\_  
 [24] BATT\_WHITE\_LED# >>> \_\_\_\_\_  
 [24] SYS\_LED\_MASK# >>> \_\_\_\_\_  
 [16] PCH\_SATA\_LED# >>> \_\_\_\_\_  
 [63] M2\_PCIE\_LED# >>> \_\_\_\_\_  
 [24,67] LID\_CL\_SIO# >>> \_\_\_\_\_  
 [24] MASK\_SATA\_LED# >>> \_\_\_\_\_

RO13\_20171001 EMI request



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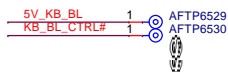
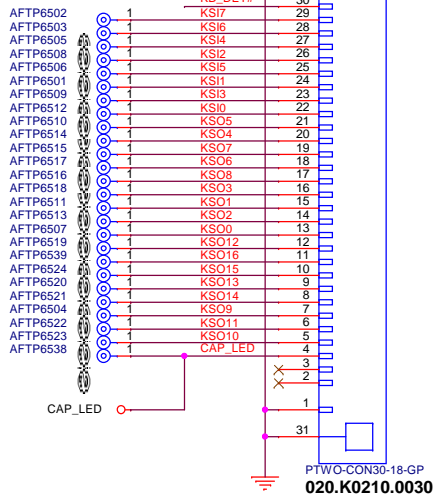
<Core Design>

<b>DELL</b>		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>LED Board&amp;Power Button</b>			
Size A4	Document Number <b>KR CS MLK 13"</b>		Rev <b>A00</b>
Date Thursday, July 19, 2018	Sheet 64		of 106

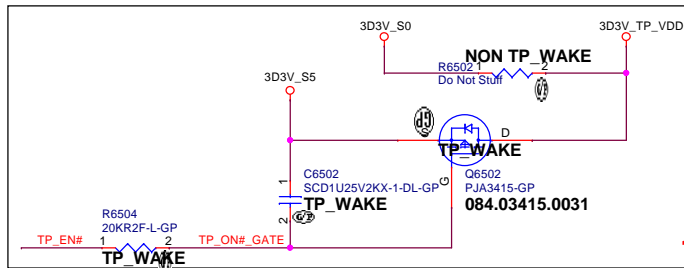
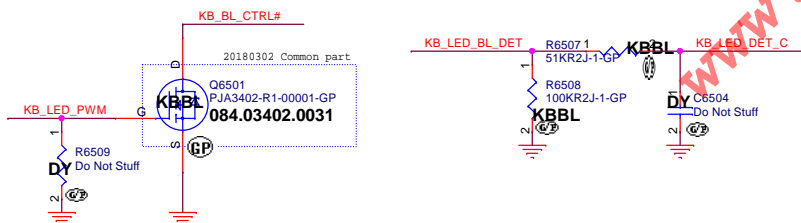
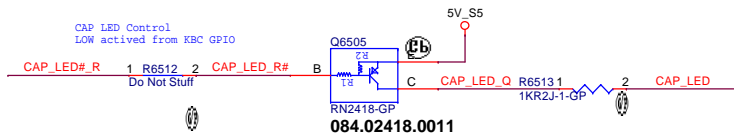
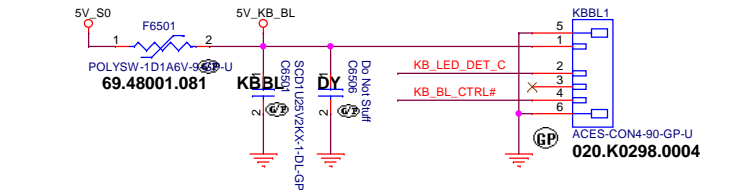


SSID = KB

## Keyboard

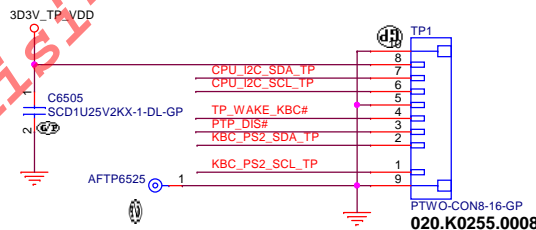
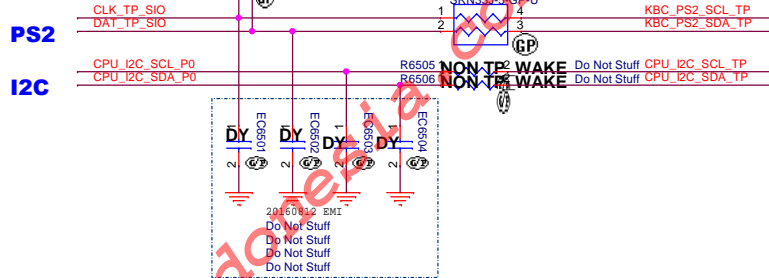


KB Backlight Power Consumption: 285mA max.



GPIO\_TPAD: TBD  
(Touch pad wake# for S3 wake up @ PCH GPIO??)

PS2  
I2C



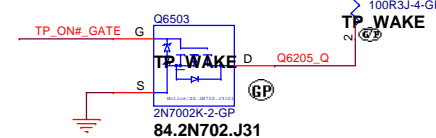
Change pindefine DVT1 0210 1330

Pin number	Pin name
1	VDD
2	DAT(I2C)
3	CLK(I2C)
4	GND
5	ATTN
6	GPIO
7	DAT(PS2)
8	CLK(PS2)

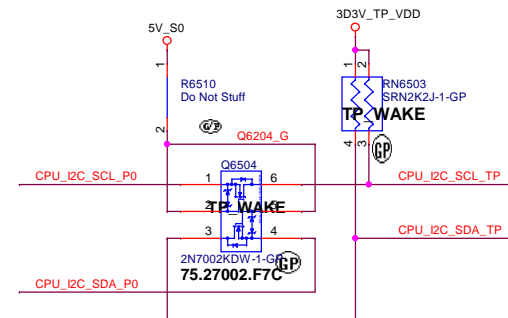
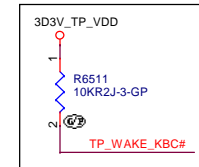
3D3V\_TP\_VDD 1 AFTP6531  
KBC\_PS2\_SCL\_TP 1 AFTP6532  
KBC\_PS2\_SDA\_TP 1 AFTP6533  
CPU\_I2C\_SCL\_TP 1 AFTP6534  
CPU\_I2C\_SDA\_TP 1 AFTP6535  
TP\_WAKE\_KBC# 1 AFTP6536  
PTP\_DIS# 1 AFTP6537

## TPAD

TP\_VDD Discharge Circuit



Need to check if it is Active High or Active Low  
and check if there is PH on TPAD side.



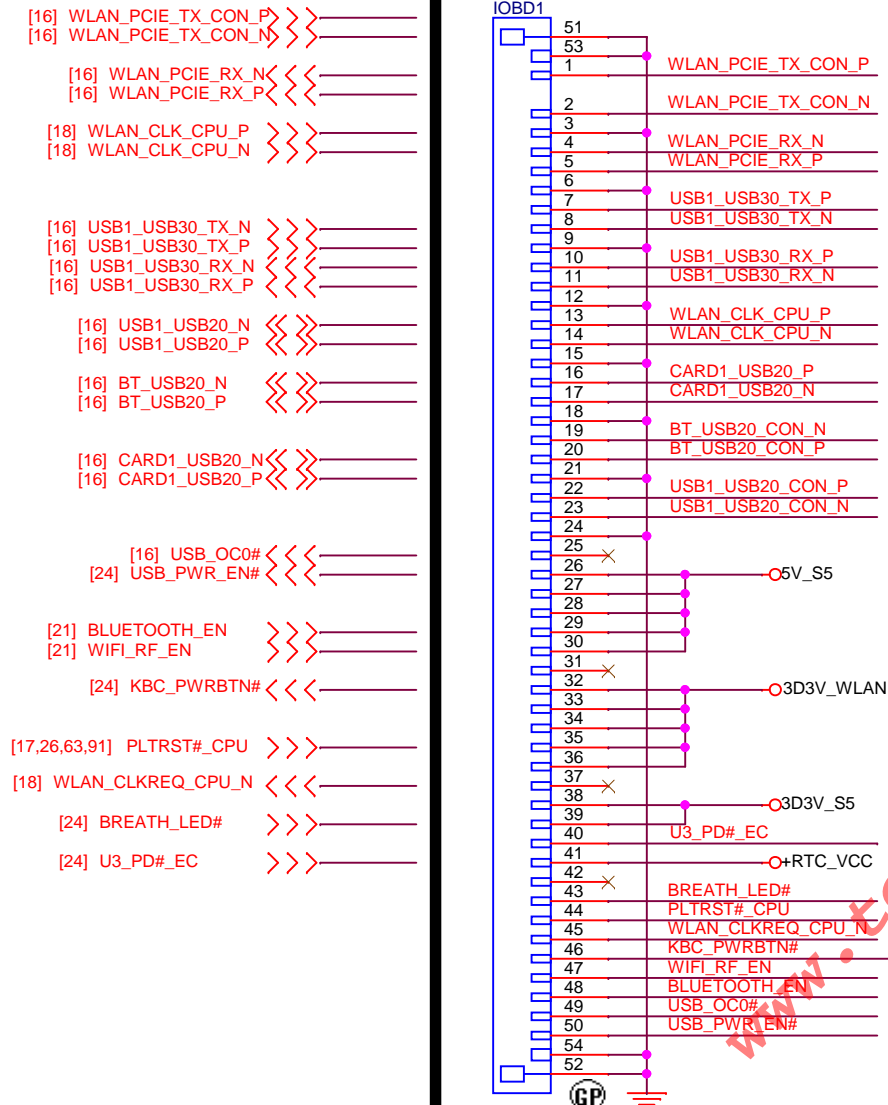
<Core Design>

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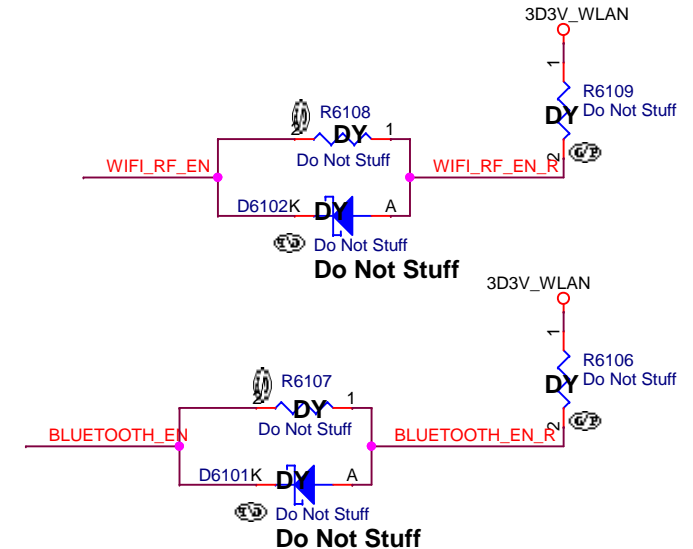
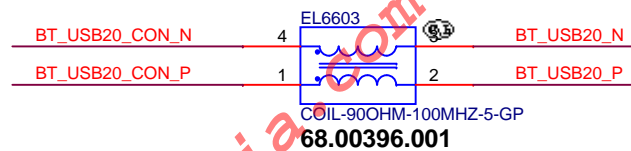
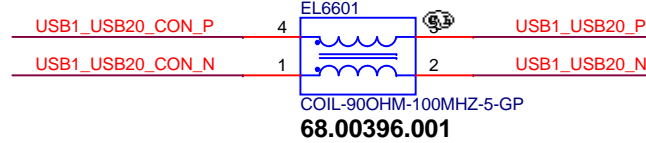
Title			
<b>Key Board&amp;Touch Pad</b>			
Size	Document Number		Rev
A3	<b>KR CS MLK 13"</b>		<b>A00</b>
Date:	Thursday, July 19, 2018	Sheet 65 of	106



# SSID = IO Connector



STAR-CON50-2-GP-U  
020.F0688.0050



KBC_PWRBTN#	1	AFTP6609
PLTRST#_CPU	1	AFTP6108
3D3V_S5	1	AFTP6607
5V_S5	1	AFTP6608
BLUETOOTH_EN	1	AFTP6112
WIFI_RF_EN	1	AFTP6110
WLAN_CLKREQ_CPU_N	1	AFTP6109
BT_USB20_CON_N	1	AFTP6111
BT_USB20_CON_P	1	AFTP6114

<Core Design>



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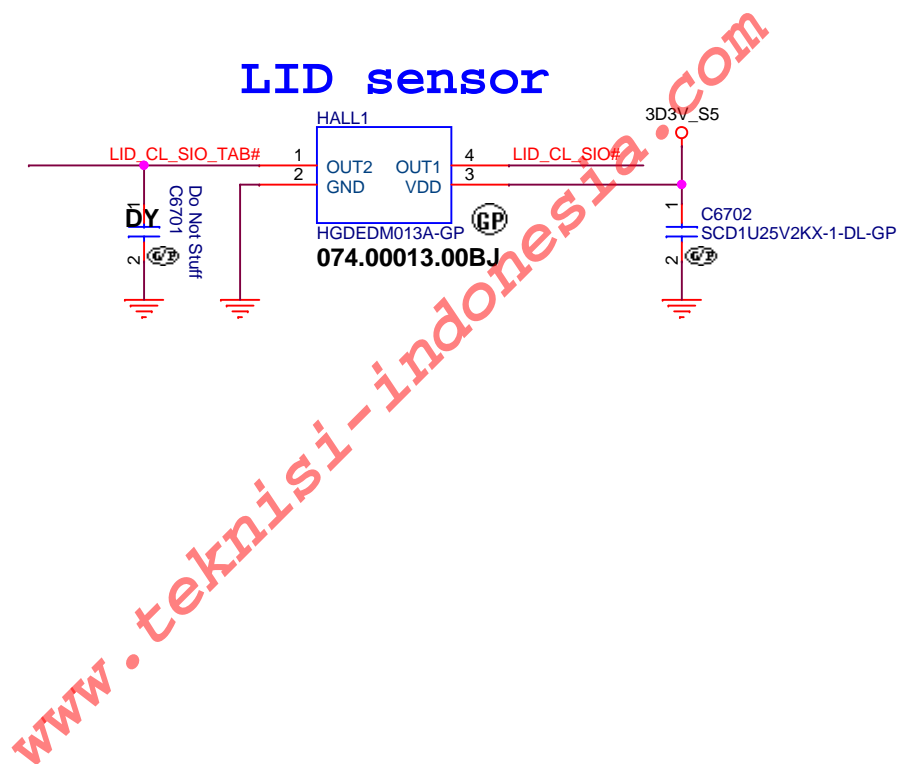
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title		
<b>IO Board Connector</b>		
Size A4	Document Number <b>KR CS MLK 13"</b>	Rev <b>A00</b>
Date: Thursday, July 19, 2018	Sheet 66	of 106




SSID = Hall Sensor

[24,64] LID\_CL\_SIO# <<<—  
[24] LID\_CL\_SIO\_TAB# <<<—

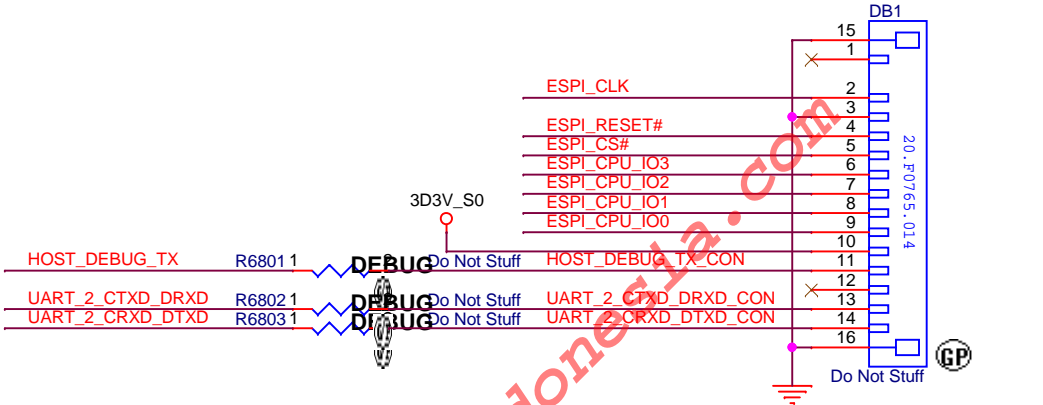
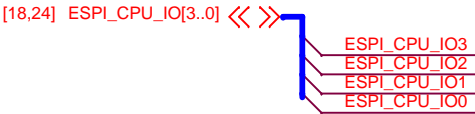


<Core Design>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>Hall Sensor</b>			
Size A4	Document Number <b>KR CS MLK 13"</b>		Rev <b>A00</b>
Date: Thursday, July 19, 2018		Sheet 67 of	106



SSID = Debug



<Core Design>

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Title <b>Dubug connector</b>			
Size A4	Document Number <b>KR CS MLK 13"</b>		Rev <b>A00</b>
Date: Thursday, July 19, 2018		Sheet 68 of 106	



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Title

***Reserved***

Size  
A4

Document Number

***KR CS MLK 13"***

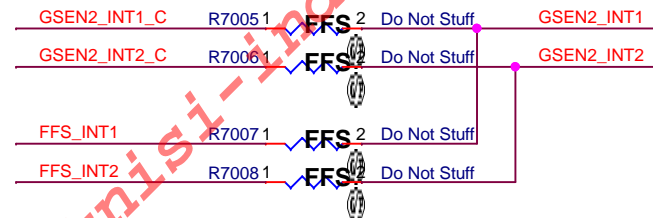
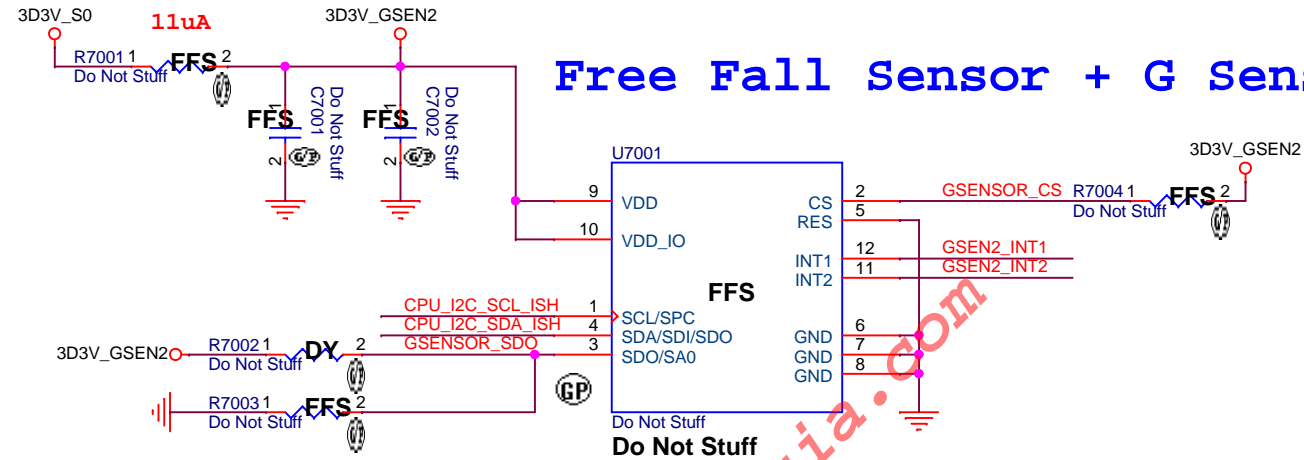
Rev  
A00

Date: Thursday, July 19, 2018

Sheet 69 of 106



## SSID = Free Fall Sensor



## <Core Design>



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Title
-------

**Sensor (G-sensor)**

Size  
A4

Document Number
-----------------

**KR CS MLK 13"**

Rev  
**AOC**

Date: Thursday, July 19, 2018

Sheet 70 of 106



# SSID = TYPEC\_MUX

## DisplayPort Source

[4] DP2\_DDI\_TX\_P0 >>>  
[4] DP2\_DDI\_TX\_N0 >>>  
[4] DP2\_DDI\_TX\_P1 >>>  
[4] DP2\_DDI\_TX\_N1 >>>  
[4] DP2\_DDI\_TX\_P2 >>>  
[4] DP2\_DDI\_TX\_N2 >>>  
[4] DP2\_DDI\_TX\_P3 >>>  
[4] DP2\_DDI\_TX\_N3 >>>

## DisplayPort HPD

[4,72] DP1\_HPD\_CPU <<<

## DisplayPort AUX

[4] DP2\_AUX\_CPU\_P >>>  
[4] DP2\_AUX\_CPU\_N >>>

## USB HOST

[73] USB1\_SBU1 >>>  
[73] USB1\_SBU2 >>>

[16] USB4\_USB30\_RX\_P <<<  
[16] USB4\_USB30\_RX\_N <<<

[16] USB4\_USB30\_TX\_P >>>  
[16] USB4\_USB30\_TX\_N >>>

## USB3.0 TYPEC CONNECTOR

[73] USB1\_SSTX\_CON\_N1 <<<  
[73] USB1\_SSTX\_CON\_P1 <<<

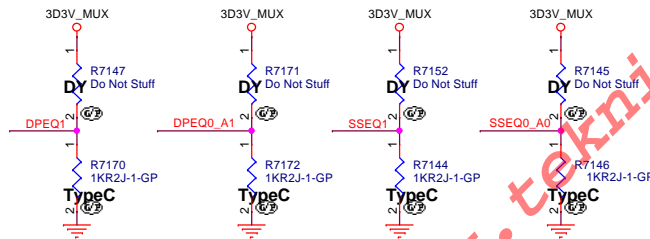
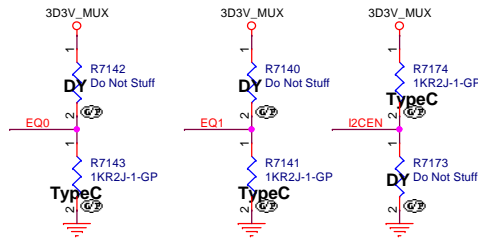
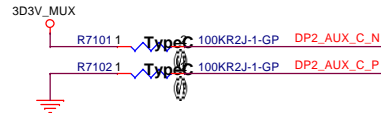
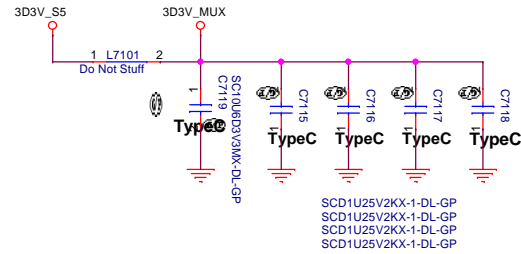
[73] USB1\_SSTX\_CON\_N2 <<<  
[73] USB1\_SSTX\_CON\_P2 <<<

[73] USB1\_SSRX\_CON\_N1 <<<  
[73] USB1\_SSRX\_CON\_P1 <<<

[73] USB1\_SSRX\_CON\_N2 <<<  
[73] USB1\_SSRX\_CON\_P2 <<<

## I2C TO PD

[72] I2C\_CLK\_PD <<<  
[72] I2C\_DATA\_PD <<<

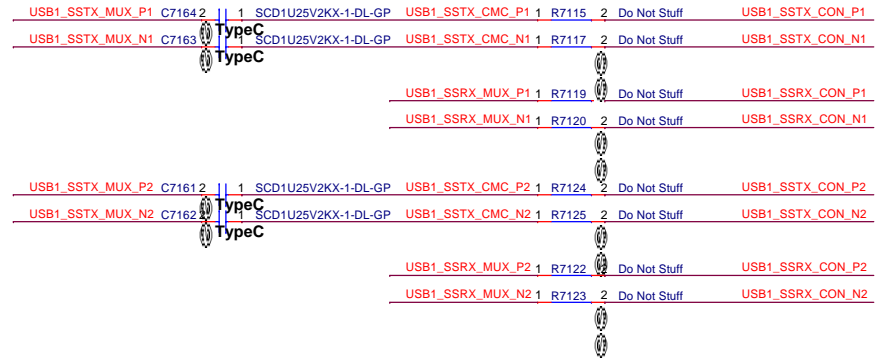
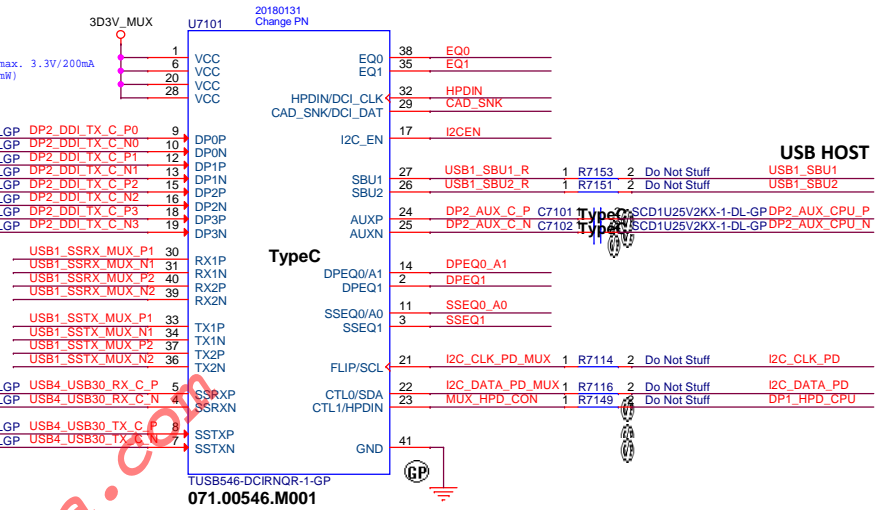
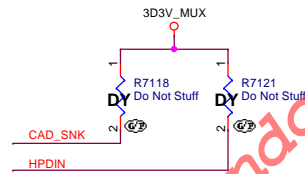


## DisplayPort Source

DP2\_DDI\_TX\_P0 C7112  
DP2\_DDI\_TX\_N0 C7113  
DP2\_DDI\_TX\_P1 C7114  
DP2\_DDI\_TX\_N1 C7107  
DP2\_DDI\_TX\_P2 C7109  
DP2\_DDI\_TX\_N2 C7108  
DP2\_DDI\_TX\_P3 C7111  
DP2\_DDI\_TX\_N3 C7110

USB1\_SSRX\_MUX\_P1 30  
USB1\_SSRX\_MUX\_N1 31  
USB1\_SSRX\_MUX\_P2 40  
USB1\_SSRX\_MUX\_N2 39  
USB1\_SSTX\_MUX\_P1 33  
USB1\_SSTX\_MUX\_N1 34  
USB1\_SSTX\_MUX\_P2 37  
USB1\_SSTX\_MUX\_N2 36

USB4\_USB30\_RX\_P C7105  
USB4\_USB30\_RX\_N C7106  
USB4\_USB30\_TX\_P C7103  
USB4\_USB30\_TX\_N C7104



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Title  
Size A3  
Document Number  
Date: Thursday, July 19, 2018  
Sheet 71 of 106  
Rev A00  
RESERVED  
KR CS MLK 13"







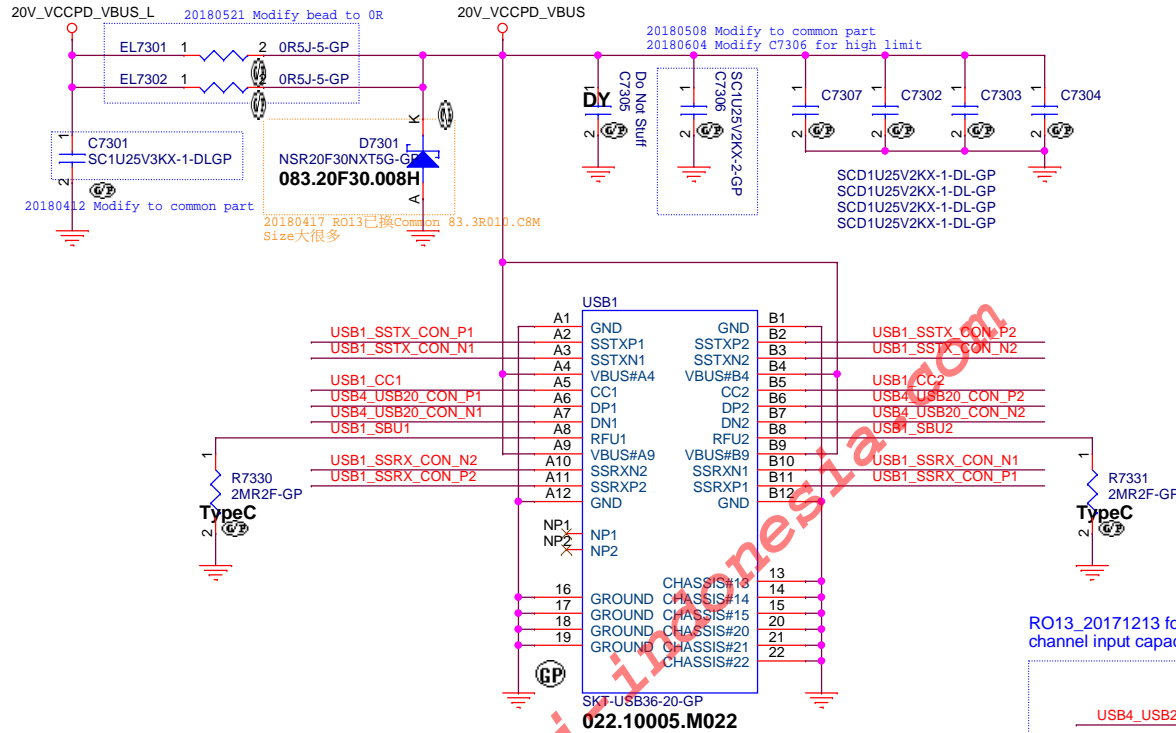
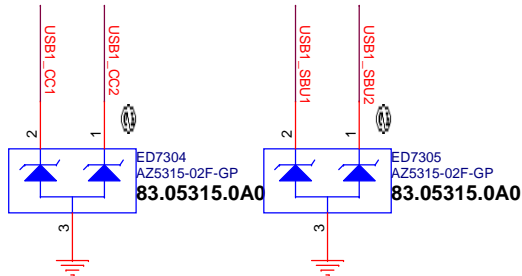
# SSID = TYPEC CONNECTOR

[71] USB1\_SSRX\_CON\_N1  
[71] USB1\_SSRX\_CON\_P1  
[71] USB1\_SSRX\_CON\_N2  
[71] USB1\_SSRX\_CON\_P2  
[71] USB1\_SSTX\_CON\_N1  
[71] USB1\_SSTX\_CON\_P1  
[71] USB1\_SSTX\_CON\_N2  
[71] USB1\_SSTX\_CON\_P2

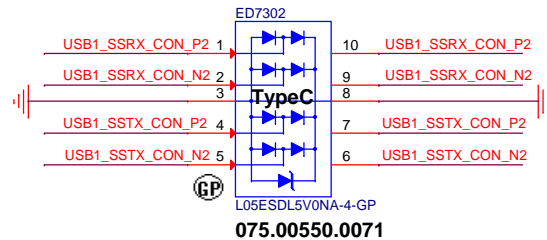
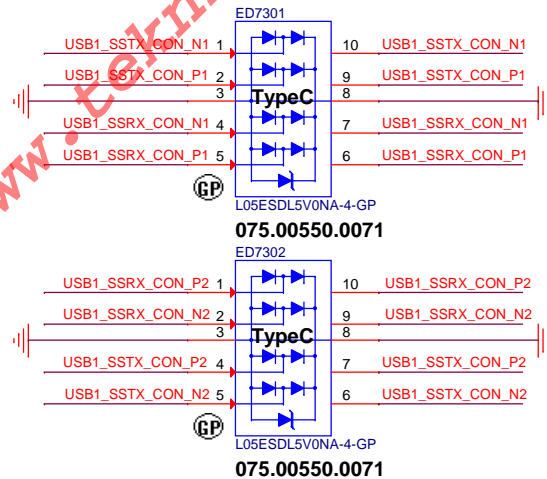
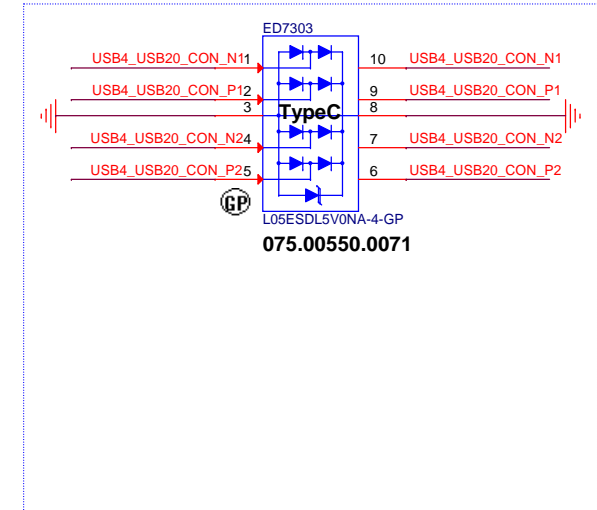
[72] USB4\_USB20\_CON\_N1  
[72] USB4\_USB20\_CON\_P1  
[72] USB4\_USB20\_CON\_N2  
[72] USB4\_USB20\_CON\_P2

[71] USB1\_SBU1  
[71] USB1\_SBU2  
[72] USB1\_CC2  
[72] USB1\_CC1

20180110 Follow RO13 to remove RX RC



RO13\_20171213 for EMI request  
channel input capacitance max.0.3pF(075.00550.0071)



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Title				
GPU(1/5)PEG				
Size	Document Number			Rev
Custom	KR CS MLK 13"			A00
Date:	Thursday, July 19, 2018	Sheet	73	of 106



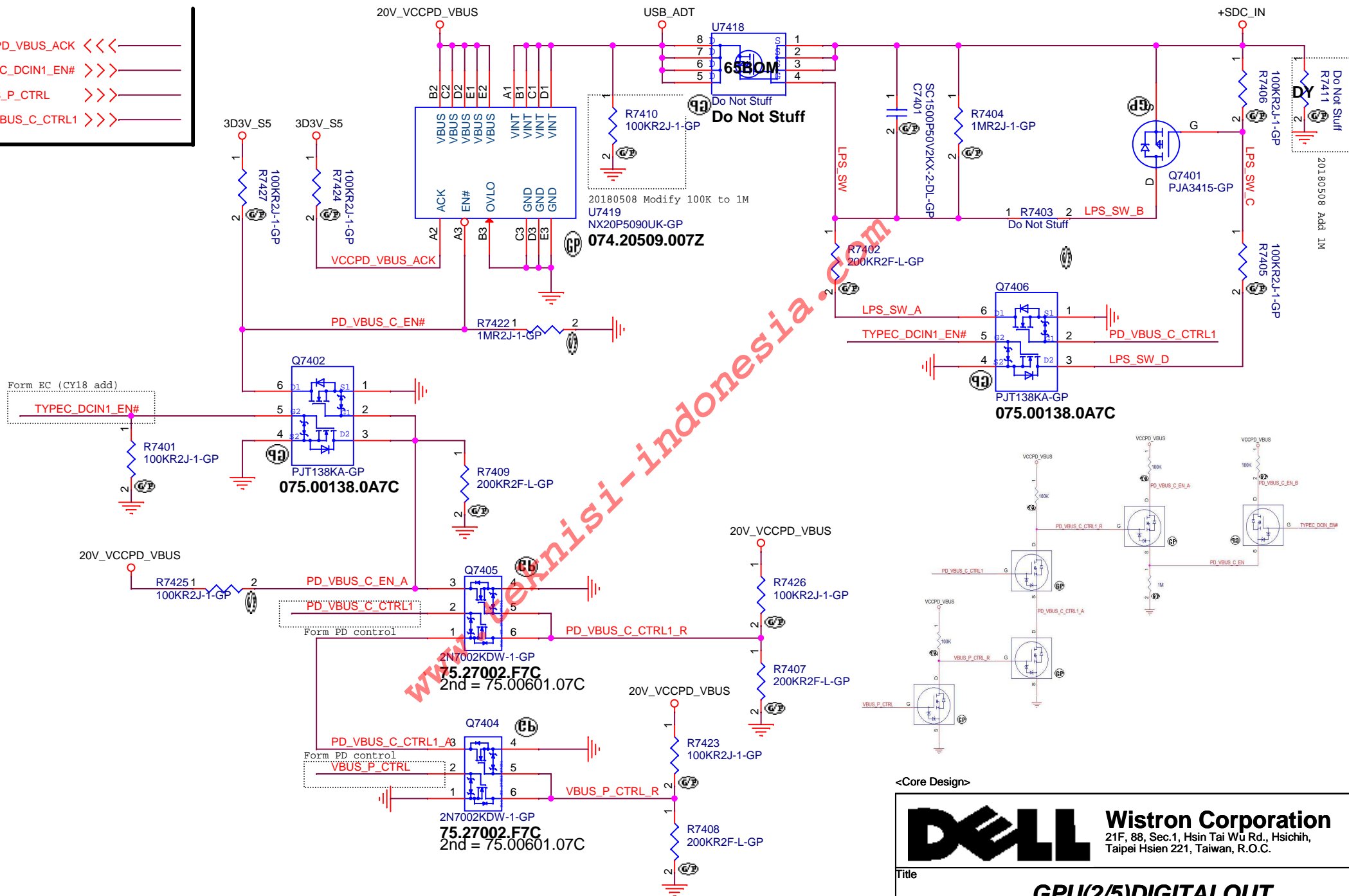
## Main Func = Type-C LPS

[44] VCCPD\_VBUS\_ACK <<< \_\_\_\_\_

[24] TYPEC\_DCIN1\_EN# >>> \_\_\_\_\_

[72] VBUS\_P\_CTRL >>> \_\_\_\_\_

[72] PD\_VBUS\_C\_CTRL1 >>> \_\_\_\_\_



## <Core Design>



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Title
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**GPU(2/5)DIGITALOUT**

Size  
A4

Document Number

**KR CS MLK 13"**

Rev  
AO

Date: Thursday, July 19, 2018

Sheet 74 of

106



Main Func = dGPU

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		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>GPU(3/5)VRAMI/F</b>			
Size A4	Document Number <b>KR CS MLK 13"</b>		Rev <b>A00</b>
Date: Thursday, July 19, 2018		Sheet 75 of	106



Main Func = dGPU

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Title

**GPU(4/5)GPIO/STRAP**

Size

Document Number

Rev

A4

**KR CS MLK 13"**

**A00**

Date: Thursday, July 19, 2018

Sheet 76 of 106



Main Func = dGPU

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Title

**GPU(5/5)PWR/GND**

Size  
A4

Document Number

**KR CS MLK 13"**

Rev

**A00**

Date: Thursday, July 19, 2018

Sheet 77 of 106




SSID = VRAM

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			<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
GPU-VRAM1,2 (1/4)					
Size	Document Number				Rev
A4	KR CS MLK 13"				A00
Date: Thursday, July 19, 2018		Sheet 78		of 106	



SSID = VRAM

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Title

**GPU-VRAM3,4 (2/4)**

Size  
A4

Document Number

**KR CS MLK 13"**

Rev  
**A00**

Date: Thursday, July 19, 2018

Sheet 79 of 106



Main Func = dGPU

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<Core Design>

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Title <b>GPU(5/5)PWR/GND</b>			
Size A4	Document Number <b>KR CS MLK 13"</b>		Rev <b>A00</b>
Date: Thursday, July 19, 2018		Sheet 80 of	106



Main Func = dGPU

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<Core Design>



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Title

**GPU-VRAM1,2 (1/4)**

Size  
A4

Document Number  
**KR CS MLK 13"**

Rev  
**A00**

Date: Thursday, July 19, 2018

Sheet 81 of 106



Main Func = dGFX\_CORE

(Blanking)

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Title

**RT8812 VGACORE**

Size  
A4

Document Number

**KR CS MLK 13"**

Rev  
**A00**

Date: Thursday, July 19, 2018

Sheet 82 of 106



Main Func = dGPU

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Title

**DISCRETE VGA POWER**

Size  
A4

Document Number

**KR CS MLK 13"**

Rev  
**A00**

Date: Thursday, July 19, 2018

Sheet 83 of 106



Main Func = dGPU

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<Core Design>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>GPU-VRAM7,8 (4/4)</b>			
Size A4	Document Number <b>KR CS MLK 13"</b>		Rev <b>A00</b>
Date: Thursday, July 19, 2018		Sheet 84 of	106



Main Func = dGFX\_CORE

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<Core Design>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>GPU CORE</b>			
Size A4	Document Number <b>KR CS MLK 13"</b>		Rev <b>A00</b>
Date: Thursday, July 19, 2018		Sheet 85 of	106




Main Func = dGPU

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Title

***GPU Discrete Power***

SizeA4

Document Number***KR CS MLK 13"***

Rev***A00***

Date: Thursday, July 19, 2018Sheet 86 of 106



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Title

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Size  
A4

Document Number

***KR CS MLK 13"***

Rev  
***A00***

Date: Thursday, July 19, 2018

Sheet 87 of 106



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Title

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Size  
A4

Document Number

***KR CS MLK 13"***

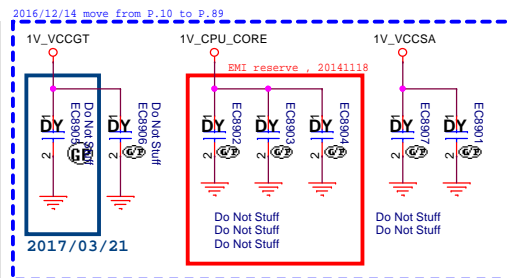
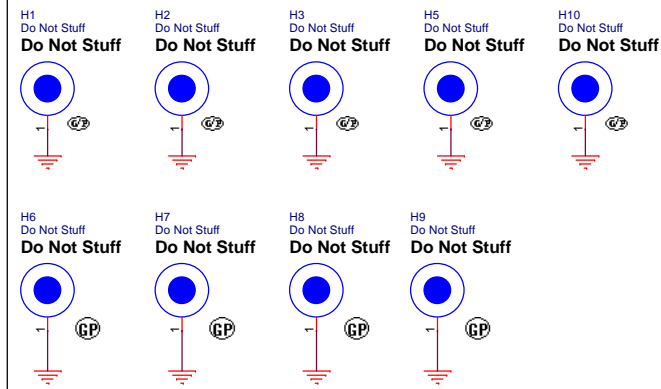
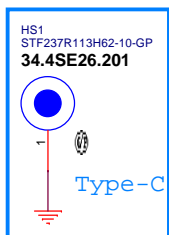
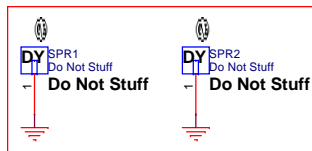
Rev  
***A00***

Date: Thursday, July 19, 2018

Sheet 88 of 106

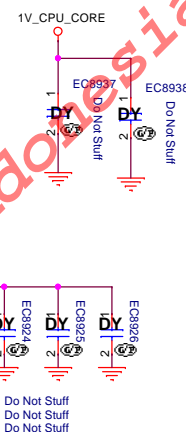
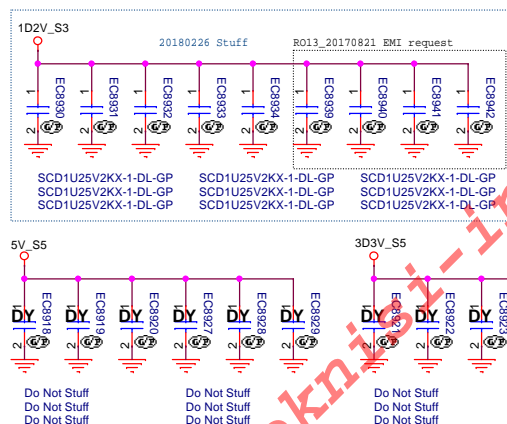
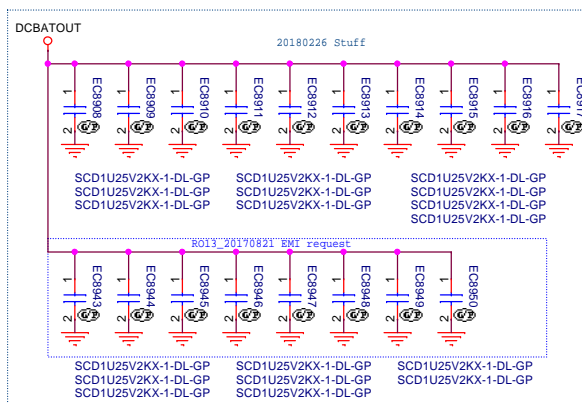


## SSID = Unused Parts



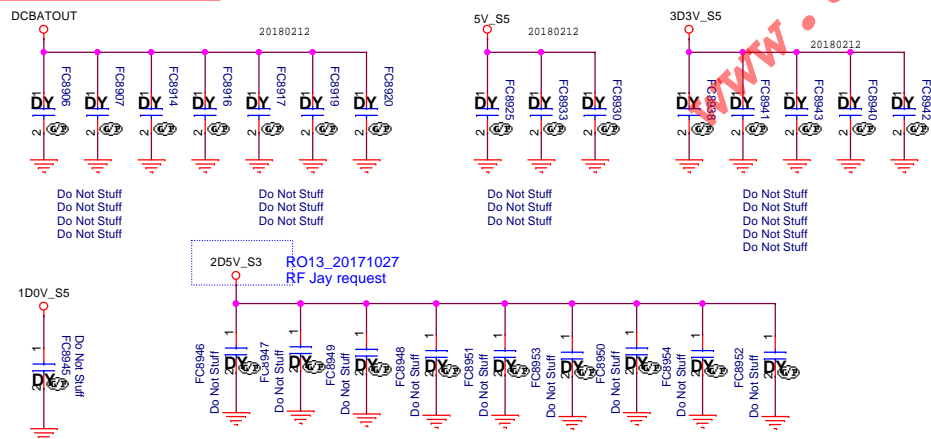
## SSID = EMI

Mind the voltage rating of the caps.



RO13\_20170821 EMI request  
RO13\_20171107 EMI request  
delete EC8951 EC8935 EC8936

## SSID = RF



<Core Design>

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Title		
UNUSED PARTS/EMI Capacitors		
Size	Document Number	Rev
A3	KR CS MLK 13"	A00
Date:	Thursday, July 19, 2018	Sheet 89 of 106



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Title

***Reserved***

Size  
A4

Document Number

***KR CS MLK 13"***

Rev  
***A00***

Date: Thursday, July 19, 2018

Sheet 90 of 106



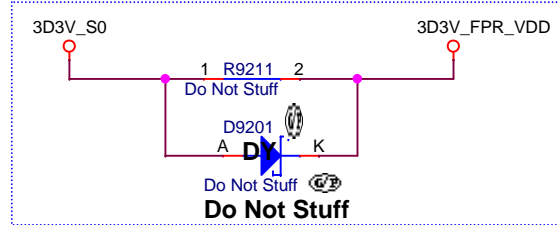




SSID = FPR

[16] FP1\_USB20\_P >>>  
[16] FP1\_USB20\_N >>>  
[24] FPR\_SCAN# >>>

20180222 Remove all SSO



## FBR(Botton side finger Print Sensor)

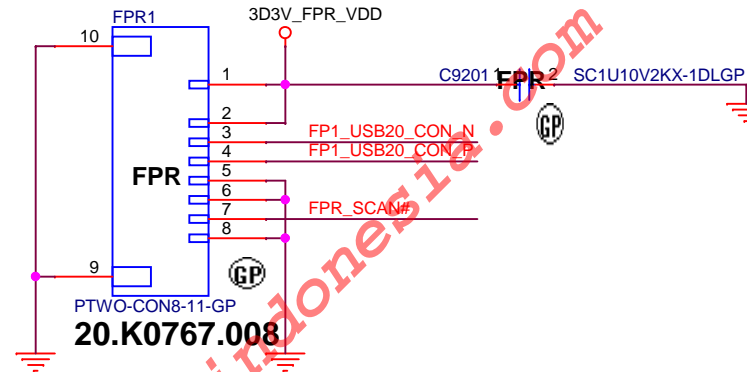
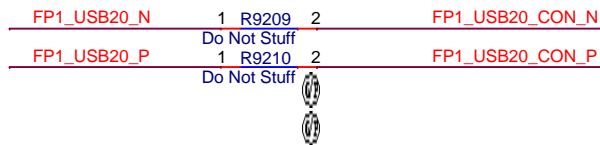
R013\_20170929  
remove R9212(DY)



### Co-lay CMC and RES

20180211

20180201 Add co-lay CMC



## GF5288WN1+GF128A+GM168 Module design

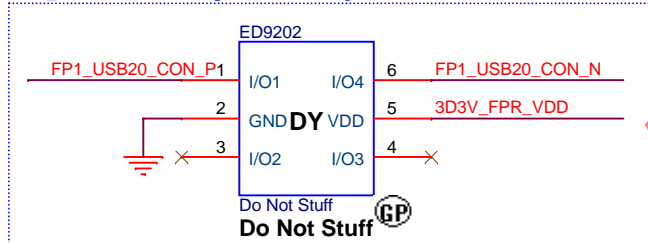
### Pin Definition

#### CN PIN MAP

PIN NO.	INFO
1	VCC-3.3V
2	Power button
3	USB_N
4	USB_P
5	GND
6	LID closed
7	GPIO_key shielding
8	GND(ID pin)

	PM_SLP_S4#	FP_3D3V
S0	1	1
S3	1	1
S4	0	0
S5	0	0

R013\_20171001 (EMI request to modify)



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Title <b>(Reserved)Finger Print</b>		
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Date: Thursday, July 19, 2018	Sheet 92 of 106	



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Rev  
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Title

**LVDS Switch**

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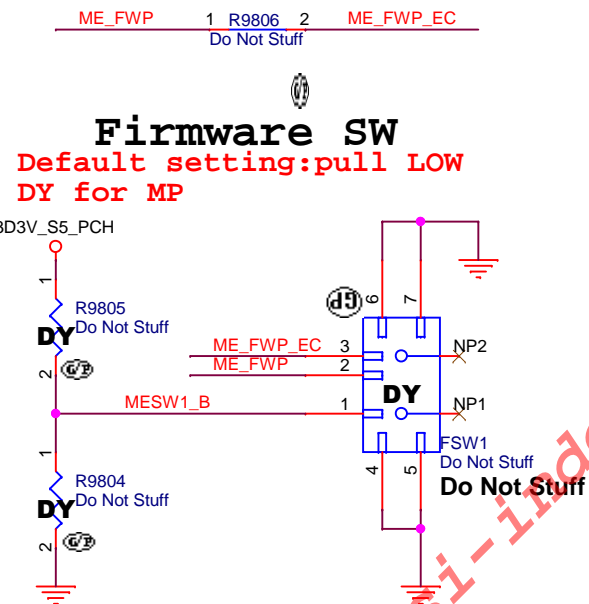
**A00**

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Sheet 97 of 106

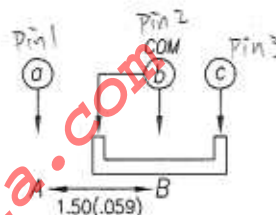


[24] ME\_FWP\_EC >>> \_\_\_\_\_  
 [19] ME\_FWP <<< \_\_\_\_\_

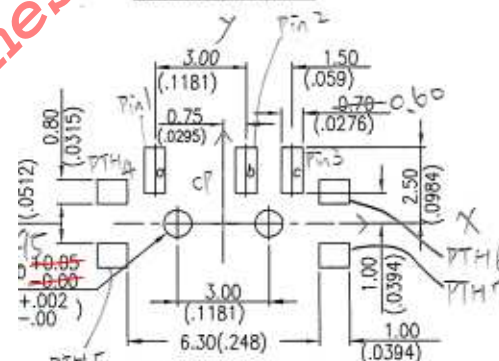


	3	1
ME_FWP	LOW	HIGH
	Normal Operation (Default)	Override

\*Symbol same as  
 62.40018.461



CIRCUIT DIAGRAM



P.C.B LAYOUT  
 Top view

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Title

**CRT Switch**

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Rev

**A00**

Date: Thursday, July 19, 2018

Sheet 98 of 106



SSID = Debug

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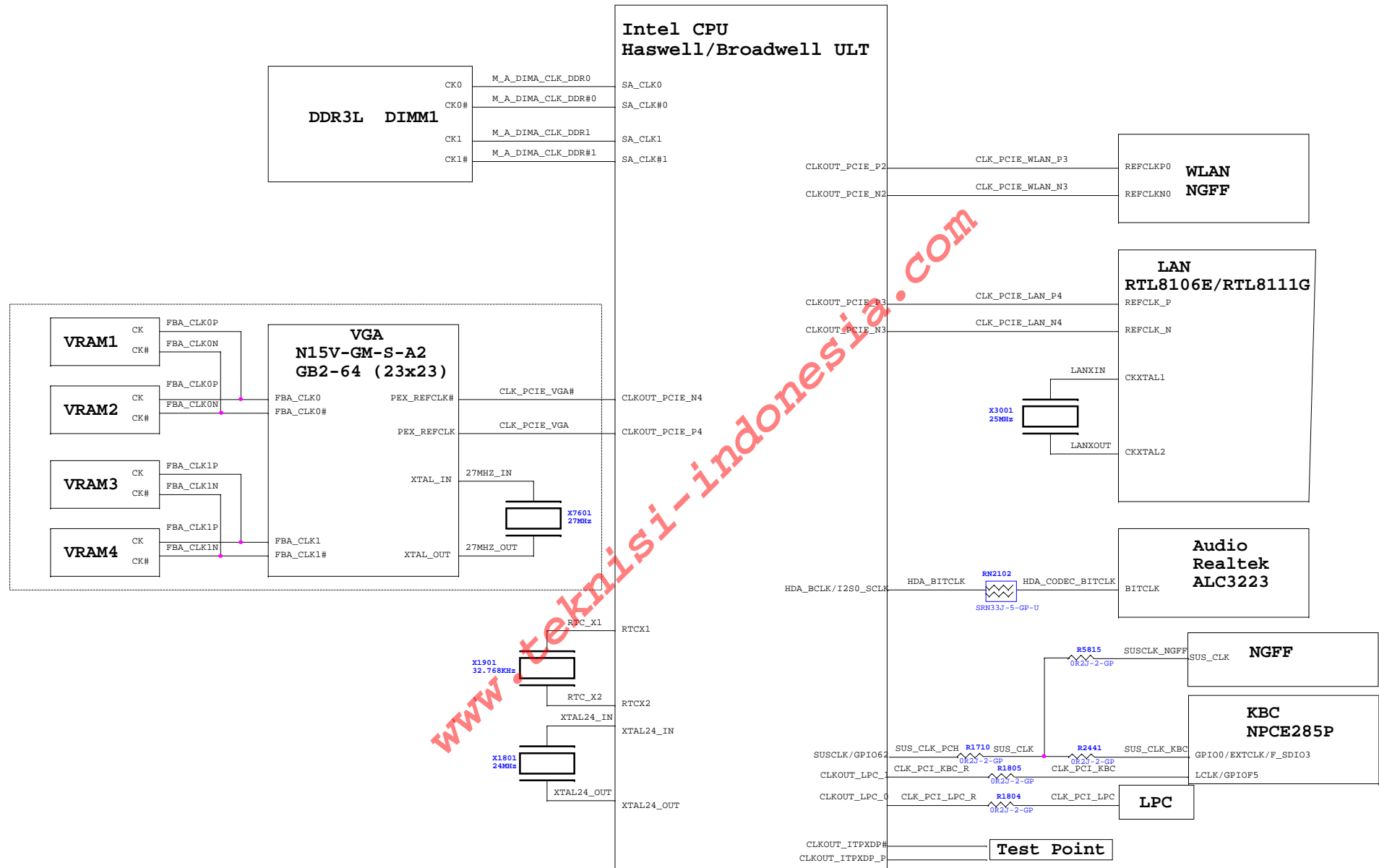
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Title <b>CPU XDP;PCH XDP</b>			
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Date: Thursday, July 19, 2018		Sheet 99	of 106



# CLK Block Diagram



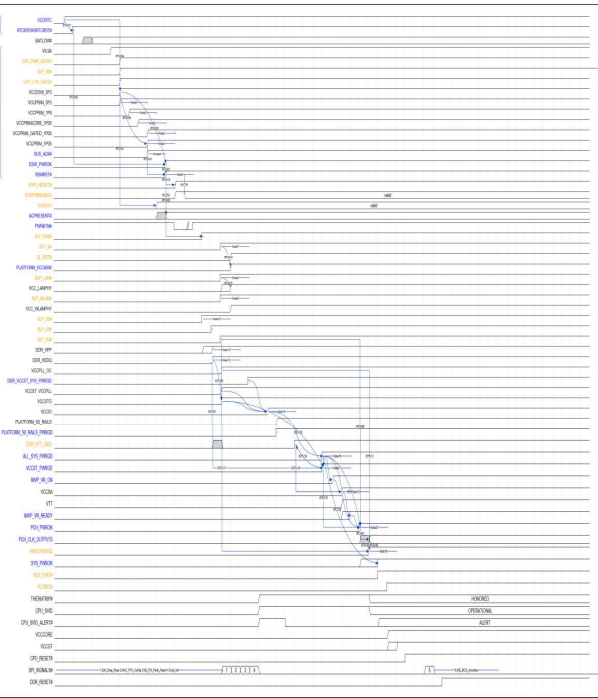


[illegible]

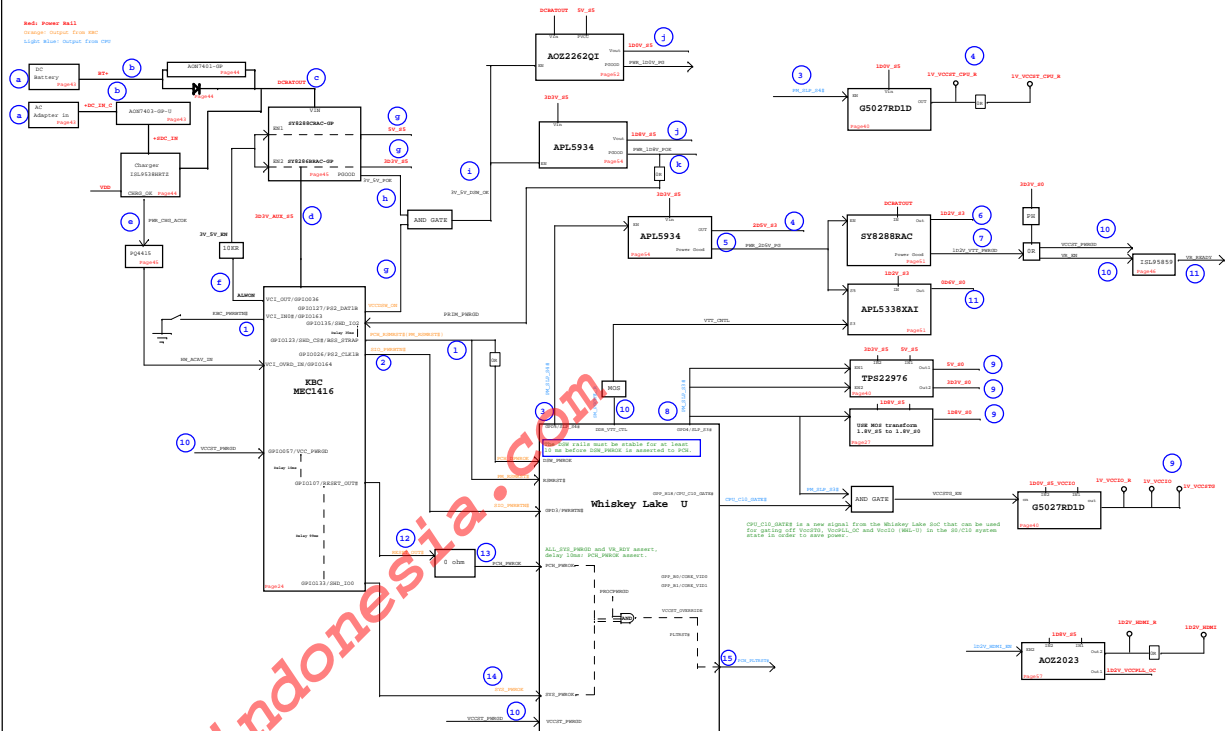
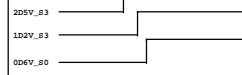
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# WHL-U Timing Diagram for G3 to S0/M0 [Non-Deep Sx Platform]



## For DDR4 power sequence

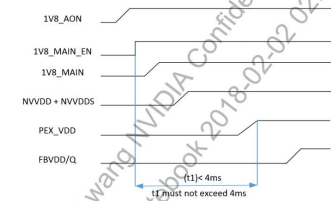


## [dGPU] N16x Power-Up/Down Sequence

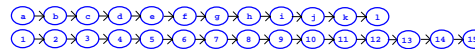
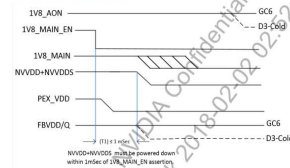
### Power-Up Sequence

- 1V8\_AON → 1V8\_MAIN → (NVVDD+NVVDD5) → PEX\_VDD → FBVDD/Q
- All CPU power rails must ramp up after 1V8\_AON
- FBVDD/Q should ramp up after (NVVDD+NVVDD5) and PEX\_VDD.

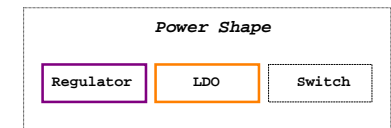
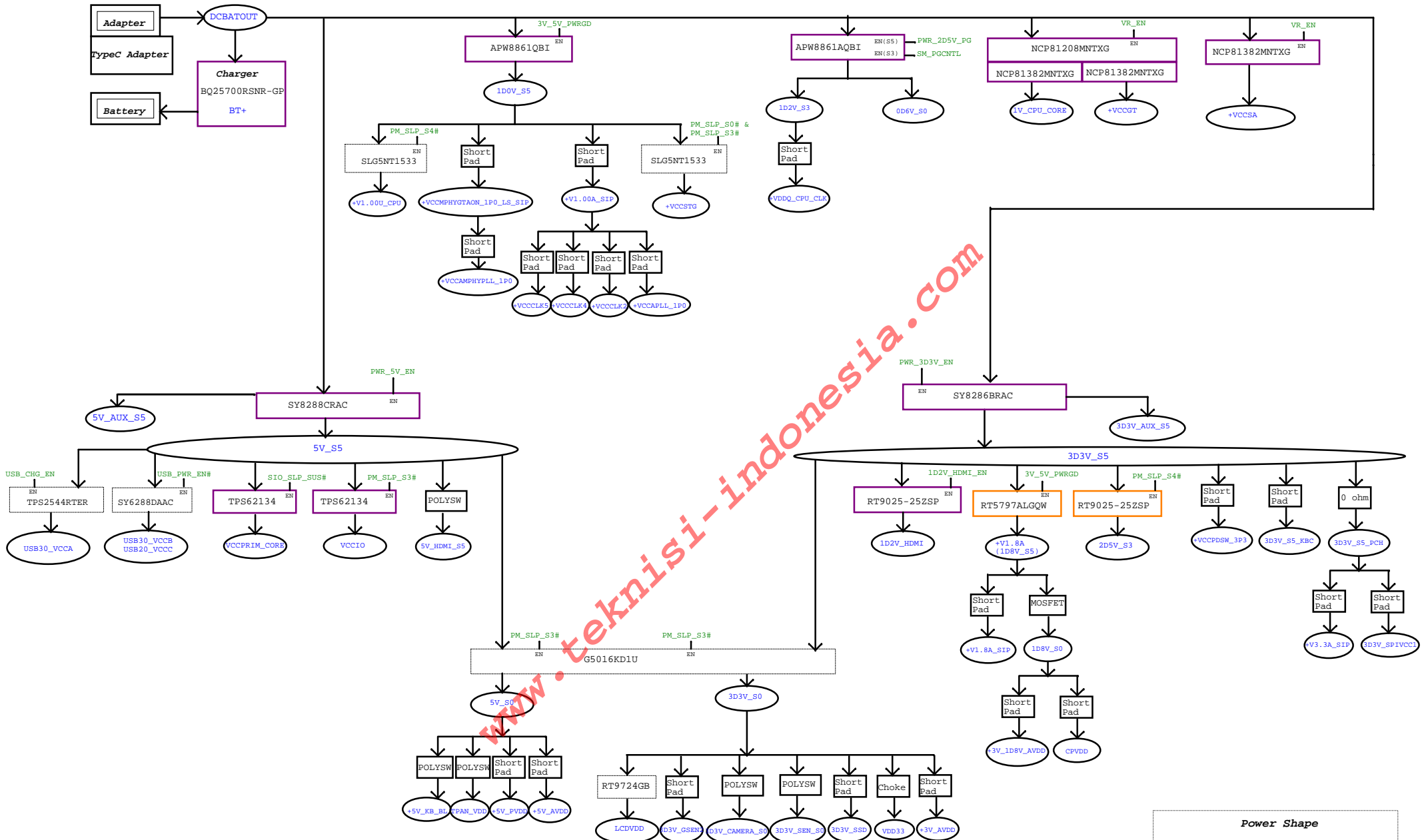
All other 1.8V power rails can ramp up with 1V8\_MAIN including PEX\_VDD and all PLLVDD rails; all other 1V power rails can ramp up with PEX\_VDD.



### Power-Down Sequence

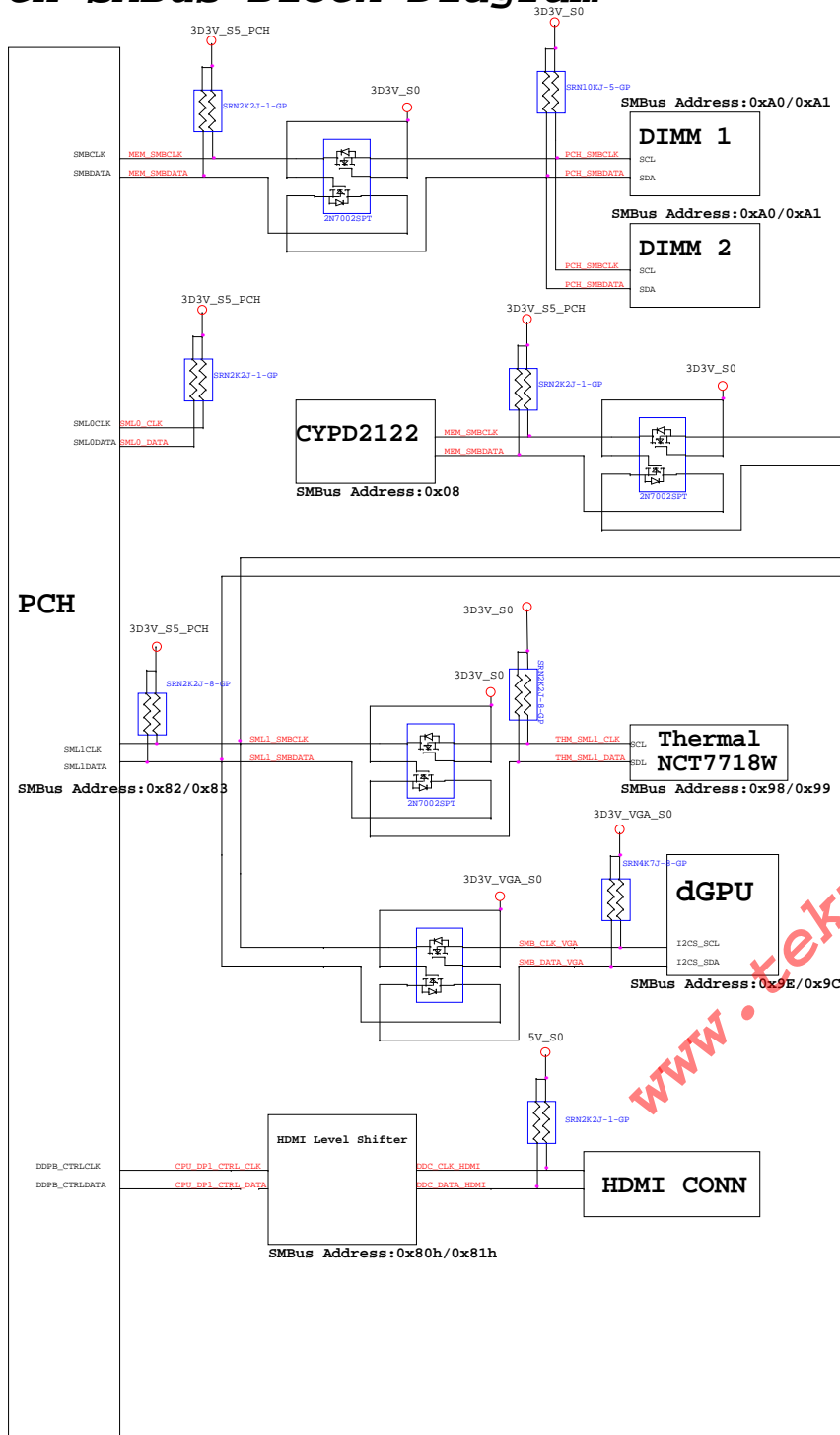




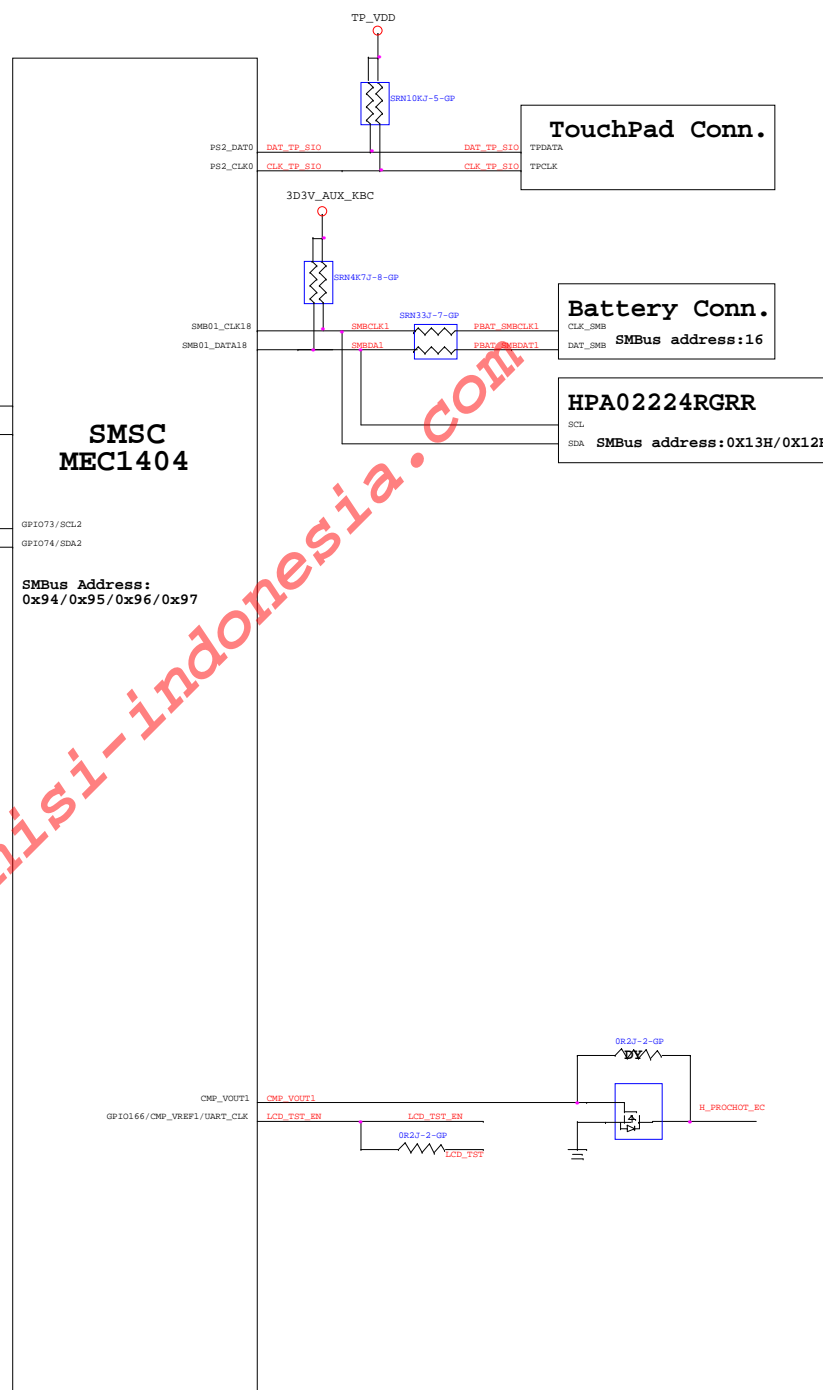




# PCH SMBus Block Diagram

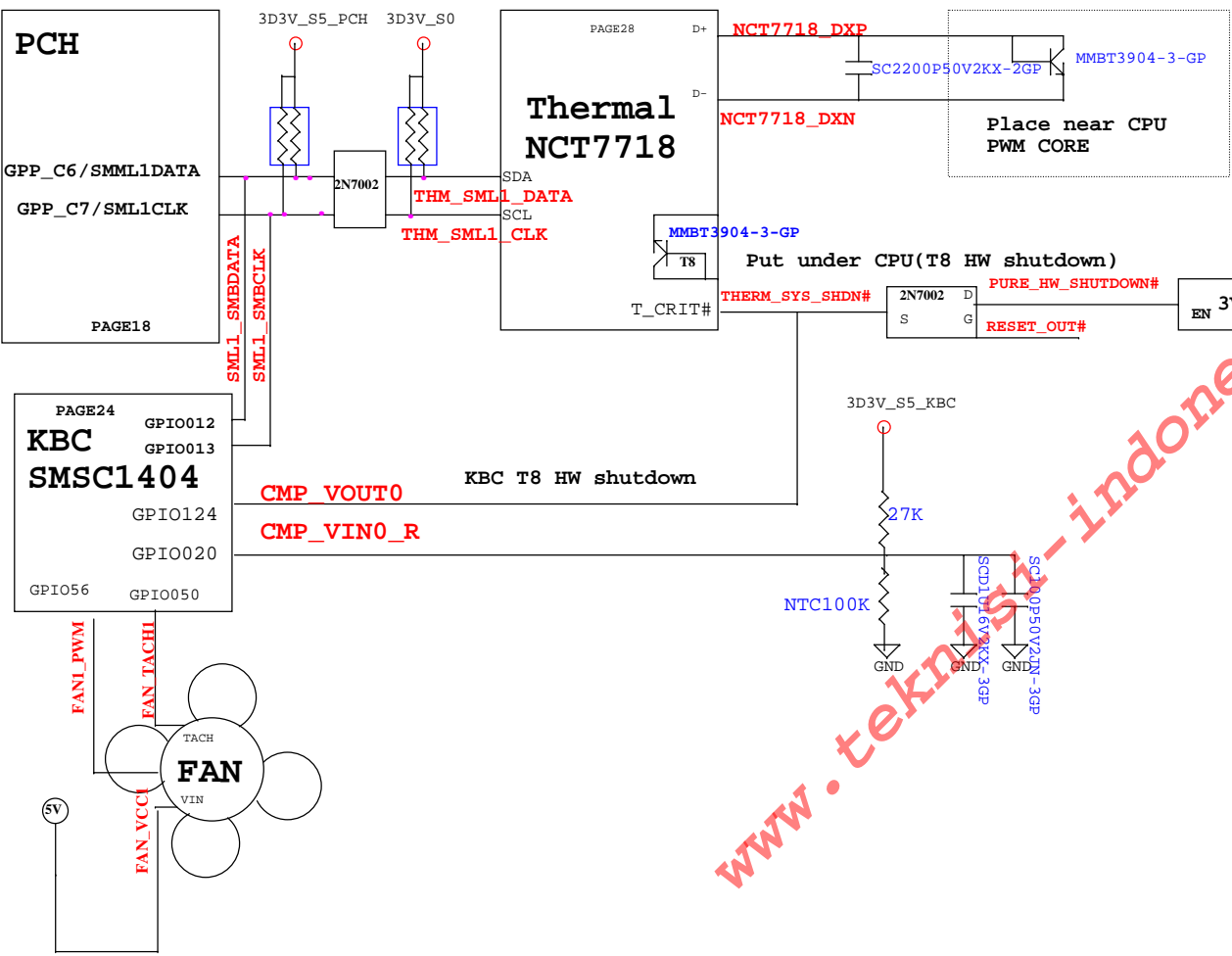


# KBC SMBus Block Diagram

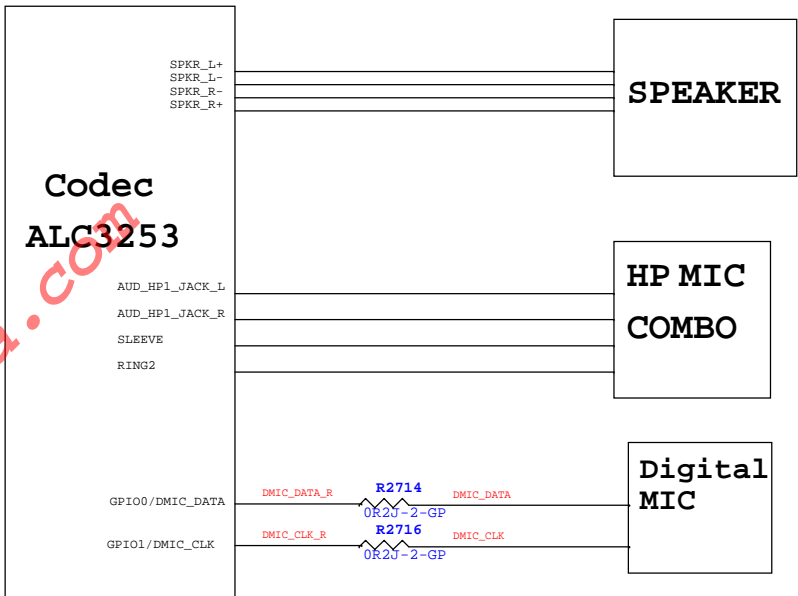




# Thermal Block Diagram



# Audio Block Diagram





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